SHARP

CIRCUIT DIAGRAM

CODE : 00ZAR650//C1/

DIGITAL COPIER

MODEL AR-650

CONTENTS

Parts marked with "⚠" are important for maintaining the safety of the set.
Be sure to replace these parts with specified ones for maintaining the safety and performance of the set.

SHARP CORPORATION

CONTENTS

GENERAL PRECAUTIONS REGARDING THE INSTALLATION AND SERVICE

The installation and service should be done by a qualified service technician.

1. Transportation/Installation

- When transporting/installing the copier, move it by the casters while lifting the stoppers.
  The copier is quite heavy and weighs approximately 250 kg (551 lb), therefore pay full attention when handling it.
- Be sure to use a dedicated outlet with AC 115V or 120V/20A (220V, 230V, 240V/10A) or more for its power source.
- The copier must be grounded for safety.
  Never ground it to a gas pipe or a water pipe.
- Select a suitable place for installation.
  Avoid excessive heat, high humidity, dust, vibration and direct sunlight.
- Also provide proper ventilation as the copier emits a slight amount of ozone.
- To insure adequate working space for the copying operation, keep a minimum clearance of 80 cm (32”) on the left, 80 cm (32”) on the right and 10 cm (4”) in the rear.

2. Service of Machines

- Basically, be sure to turn the main switch off and unplug the power cord during service.
- Be sure not to touch high-temperature sections such as the exposure lamp, the fuser unit, the damp heater and their periphery.
- Be sure not to touch high-voltage sections such as the chargers, the transfer belt and the high-voltage transformer.
- Be sure not to touch rotating/operating sections such as gears, belts, pulleys, fan, etc.
- When servicing the machines with the main switch turned on, be sure not to touch live sections and rotating/operating sections. Avoid exposure to laser radiation.
- Use suitable measuring instruments and tools.
- Avoid exposure to laser radiation during servicing.
  - Avoid direct exposure to beam.
  - Do not insert tools, parts, etc. that are reflective into the path of the laser beam.
  - Remove all watches, rings, bracelets, etc. that are reflective.

3. Main Service Parts for Safety

- The breaker, door switch, fuse, thermostat, thermofuse, thermistor, etc. are particularly important for safety. Be sure to handle/install them properly.

4. Cautionary Labels

- During servicing, be sure to check the rating plate and the cautionary labels such as “Unplug the power cord during service”, “Hot area”, “Laser warning label” etc. to see if there is any dirt on their surface and whether they are properly stuck to the copier.

5. **Disposition of Consumable Parts/Packing Materials**
   - Regarding the recovery and disposal of the copier, supplies, consumable parts and packing materials, it is recommended to follow the relevant local regulations or rules.

6. **When parts are disassembled, reassembly is basically the reverse of disassembly unless otherwise noted in this manual or other related documents. Be careful not to reassemble small parts such as screws, washers, pins, E-rings, toothed washers in the wrong places.**

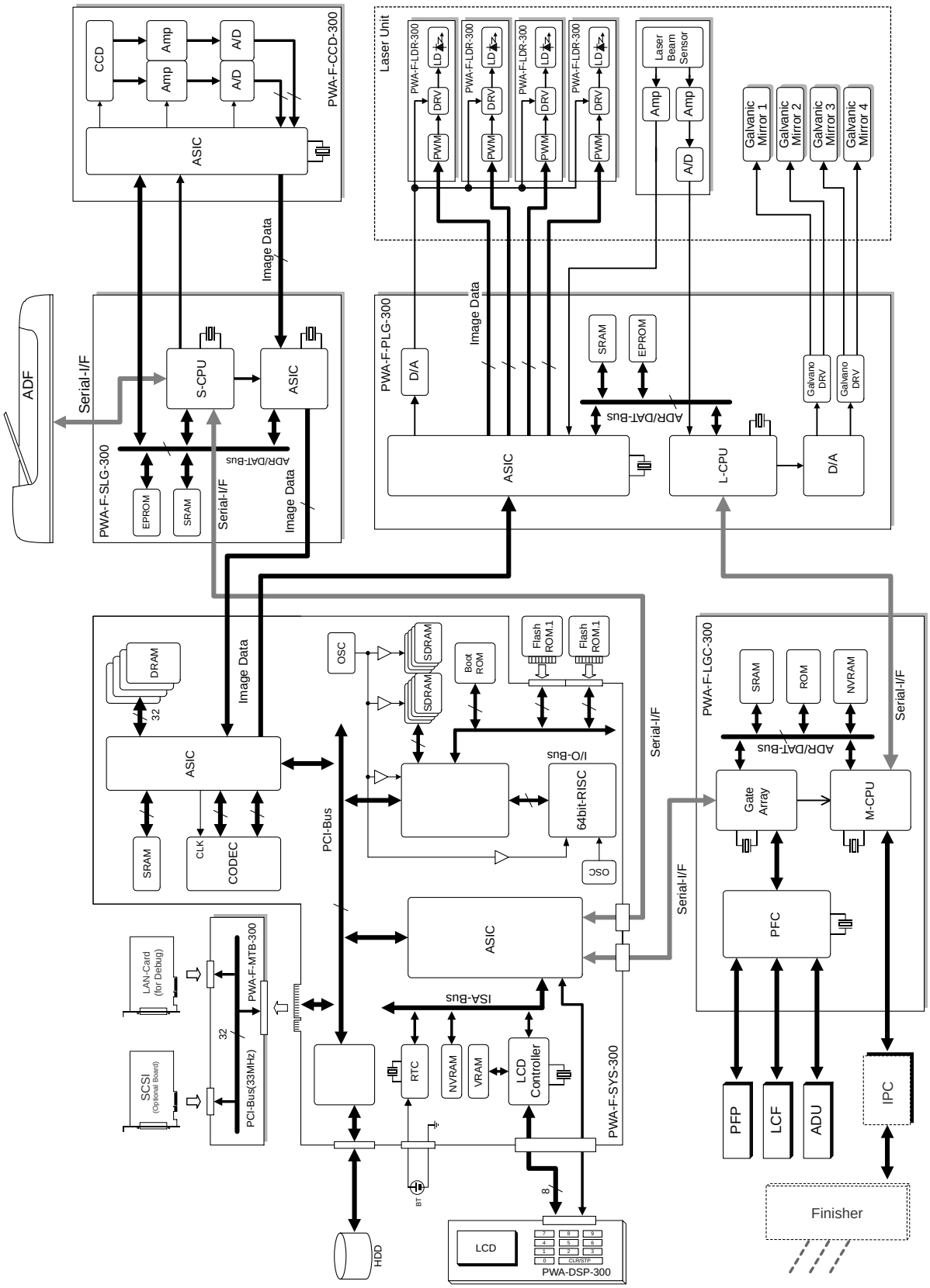
7. **Basically, the machine should not be operated with any parts removed or disassembled.**

8. **Precautions Against Static Electricity**
   - The PC board must be stored in an anti-electrostatic bag and handled carefully using a wrist-band, because the ICs on it may become damaged due to static electricity.

   Caution: Before using the wrist band, pull out the power cord plug of the copier and make sure that there is no uninsulated charged objects in the vicinity.

Caution	**:**	Dispose of used RAM-IC's (including lithium battery) according to the manufacturer's instructions.
Vorsicht	**:**	Entsorgung des gebrauchten RAM-IC's (inklusive der Lithium Batterie) nach Angaben des Herstellers.

1. DESCRIPTION OF CIRCUIT



1.1 CPU Functions

1.1.1 Main CPU (TMP95C063F)

(1) Outline and Features

The main CPU is a high-speed, advanced-function 16-bit microcontroller. This 144-pin mini flat package microcontroller has been developed for control of various mid-scale to large-scale equipment.
The main features of the main CPU are as follows:

① Original high-speed 16-bit CPU (900H_CPU)
- Upwardly compatible with TLCS-90/900 and instruction mnemonics
- 16 Mbyte linear address space
- General-use register and register bank system
- 16-bit multiplication and division operations, bit transfer/operation instructions
- High-speed DMA: 4-channel (640 ns/2 bytes at 25 MHz)

② Minimum instruction execution time: 160 ns (at 25 MHz oscillation)

③ Built-in RAM: Not available
Built-in ROM: Not available

④ External memory expansion
- Expandable to 16 Mbytes (both for program/data)
- External data bus width select terminal (AM8/16)
- Coexistence of external data bus 8/16 bit widths possible
  ... Dynamic data bus sizing

⑤ Built-in DRAM controller: 2 ch
- $\overline{2CAS}$/$\overline{2WE}$ selectable

⑥ 8-bit timer: 8 ch

⑦ 16-bit timer: 2 ch

⑧ Pattern generator: 4-bit x 2 ch

⑨ General-use serial interface: 2 ch
- Baud rate generated by external clock

⑩ 10-bit A/D converter: 8 ch

⑪ 8-bit D/A converter: 2 ch

⑫ Watchdog timer

⑬ Chip select/wait controller: 4 blocks

⑭ Interrupt functions
- CPU x 2: Software interrupt instructions, undefined instruction violation
- Internal interrupts: x 22
- External interrupts: x 11

} Seven interrupt masking levels can be set.

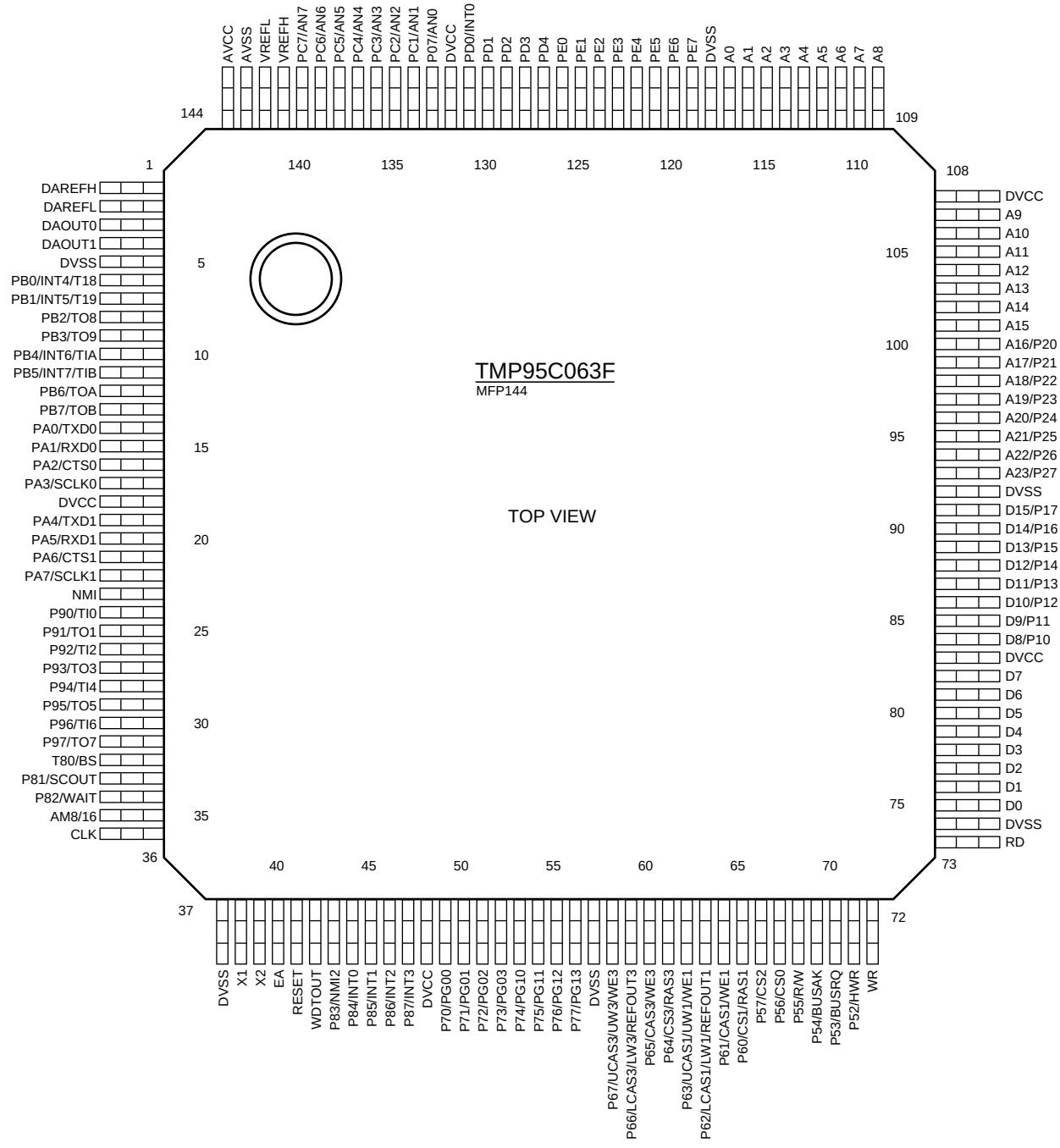
⑮ 91 I/O port terminals

⑯ Standby function
Three halt modes (RUN, IDLE, STOP)

(2) Main CPU functions

The main CPU has respective interfaces with system CPU, PFC, engine gatearray, finisher interface IC (IPC), laser CPU for each, and performs the entire control of the copier engine.
The control program is stored in external ROM (27C4002-100F1).
Adjustment values for the engine are stored in battery backed up externel RAM (NVM).

(3) Pin assignments



Pin assignment diagram (top view)

I/O Map of Main CPU

Port Name	At reset	R	IN/OUT	Signal Name	FUNCTION
P97/T07	CMOS-IN PULL-UP	X	IN	FCOV-1	Front cover, H: Open, L:Close
P96/T16	CMOS-IN PULL-UP	X	IN	TRNSW-0	Reverse switch H: When paper is past, L: No paper, (TRN-SW:S18)
P95/T05	CMOS-IN PULL-UP	X	IN	TRNES-0	Reverse exit switch, H: When paper is past, L: No paper, (TRNE-SW:S17)
P94/T14	CMOS-IN PULL-UP	—	OUT	POUT-0	External I/F output (image quality control)
P93/T03	CMOS-IN PULL-UP	X	IN	TFUSW-1	A toner full: H, Normal: L, (T-FULL-SW:SW15)
P92/T12	CMOS-IN PULL-UP	X	IN	EINT1-1	External I/F input 2 (image quality control)
P91/T01	CMOS-IN PULL-UP	X	IN	EXTSW-1	Fuser exit switch, L: When paper is past, H: No paper, (EXIT-SW:S15)
P90/T10	CMOS-IN PULL-UP	—	OUT	MVDEN-1	Paper transport signal to POPS on PLG board
P87/INT3	CMOS-IN PULL-UP	↑	IN	TXINT-1	MAIN⇔PC communications interrupt
P86/INT2	CMOS-IN PULL-UP	↑	IN	CMINT-1	MAIN⇔System-CPU(S) reception interrupt
P85/INT1	CMOS-IN PULL-UP	↑	IN	PFREQ-1	PFC→MAIN reception request interrupt
P84/INT0	CMOS-IN PULL-UP	X	IN	EINT2-1	External I/F input 3 (image quality control)
P83/NMI2	CMOS-IN PULL-UP	—	Not used		
P82/WAIT	CMOS-IN PULL-UP	—	OUT	CTDRM-0	Image density sensor (IQM) REM signal, L:ON, H:OFF
P81/SCOUT	CMOS-IN PULL-UP	↑	IN	LSBSY-1	L-CPU operation status signal
P80/BS	CMOS-IN PULL-UP	X	IN	DEVSW-0A	Developer unit, L: Installed, H: Uninstalled
P77/PG13	CMOS-IN PULL-UP	—	OUT	TRMD-0	Transfer belt motor driving signal (Low active),(TRB-MOT:M25)
P76/PG12	CMOS-IN PULL-UP	—	OUT	TRMC-0	
P75/PG11	CMOS-IN PULL-UP	—	OUT	TRMB-0	
P74/PG10	CMOS-IN PULL-UP	—	OUT	TRMA-0	
P73/PG03	CMOS-IN PULL-UP	—	OUT	RGTD-0	Alingning motor driving signal (Low active), (RGT-MOT:M17)
P72/PG02	CMOS-IN PULL-UP	—	OUT	RGTC-0	
P71/PG01	CMOS-IN PULL-UP	—	OUT	RGTB-0	
P70/PG00	CMOS-IN PULL-UP	—	OUT	RGTA-0	
P67/UCAS3/UW3/WE3	TTL-OUT H	—	Not used		
P66/LCAS3/LW3/REFOUT	TTL-OUT H	—	Not used		
P65/CAS3/WE3	TTL-OUT H	—	OUT		
P64/CS3/RAS3	TTL-OUT H	—	OUT	CS3-0	Chip select for SRAM

Port Name	At reset	R	IN/OUT	Signal Name	FUNCTION
P63/UCAS1/UW1/ WE1	TTL-OUT H	—	Not used		
P62/LCAS1/LW1/ REFOUT1	TTL-OUT H	—	Not used		
P61/CAS1/WE1	TTL-OUT H	—	Not used		
P60/CS1/RAS1	TTL-OUT H	—	OUT	CS1-0	Finisher IPC chip select
P57/CS2	TTLOUT L	—	OUT	CS2-0	Main ROM chip select
P56/CS0	TTL-OUT H	—	OUT	CS0-0	Gate array chip select
P55/RW	CMOS-IN PULL-UP	—	OUT	RW-0	Optional interface switching control signal
P54/BUSAK	CMOS-IN PULL-UP	—	OUT	STKCL-0	Stack clutch, L:ON, H:OFF, (STK-CLT:CL3)
P53/BUSRQ	CMOS-IN PULL-UP	—	OUT	REVCL-0	Reverse clutch, L:ON, H:OFF, (REV-CLT:CL2)
P52/HWR	CMOS-IN PULL-UP	X	IN	EINT3-1	External I/F input 4 (image quality control)
WR		—	OUT	WR-0	External memory write signal
RD		—	OUT	RD-0	External memory read signal
P27/A23	TTL-OUT H	—	OUT	ERSLP-0	Discharge LED lamp, L:ON, H:OFF, (ERS)
P26/A22	TTL-OUT H	—	Not used		
P25/A21	TTL-OUT H	—	OUT	A21	Address bus
P24/A20	TTL-OUT H	—	OUT	A20	Address bus
P23/A19	TTL-OUT H	—	OUT	WD-E	WD-E signal, Enable:H, Disable:L
P22/A18	TTL-OUT H	—	OUT	A18	Address bus
P21/A17	TTL-OUT H	—	OUT	A17	Address bus
P20/A16	TTL-OUT H	—	OUT	A16	Address bus
P17/D15	TTL 3STATE	—	IN/OUT	D15	Data bus
P16/D14	TTL 3STATE	—	IN/OUT	D14	Data bus
P15/D13	TTL 3STATE	—	IN/OUT	D13	Data bus
P14/D12	TTL 3STATE	—	IN/OUT	D12	Data bus
P13/D11	TTL 3STATE	—	IN/OUT	D11	Data bus
P12/D10	TTL 3STATE	—	IN/OUT	D10	Data bus
P11/D9	TTL 3STATE	—	IN/OUT	D9	Data bus
P10/D8	TTL 3STATE	—	IN/OUT	D8	Data bus
D7	TTL 3STATE	—	IN/OUT	D7	Data bus
D6	TTL 3STATE	—	IN/OUT	D6	Data bus
D5	TTL 3STATE	—	IN/OUT	D5	Data bus
D4	TTL 3STATE	—	IN/OUT	D4	Data bus
D3	TTL 3STATE	—	IN/OUT	D3	Data bus
D2	TTL 3STATE	—	IN/OUT	D2	Data bus
D1	TTL 3STATE	—	IN/OUT	D1	Data bus

Port Name	At reset	R	IN/OUT	Signal Name	FUNCTION
D0	TTL 3STATE	—	IN/OUT	D0	Data bus
A15	TTL OUT	—	OUT	A15	Address bus
A14	TTL OUT	—	OUT	A14	Address bus
A13	TTL OUT	—	OUT	A13	Address bus
A12	TTL OUT	—	OUT	A12	Address bus
A11	TTL OUT	—	OUT	A11	Address bus
A10	TTL OUT	—	OUT	A10	Address bus
A9	TTL OUT	—	OUT	A9	Address bus
A8	TTL OUT	—	OUT	A8	Address bus
A7	TTL OUT	—	OUT	A7	Address bus
A6	TTL OUT	—	OUT	A6	Address bus
A5	TTL OUT	—	OUT	A5	Address bus
A4	TTL OUT	—	OUT	A4	Address bus
A3	TTL OUT	—	OUT	A3	Address bus
A2	TTL OUT	—	OUT	A2	Address bus
A1	TTL OUT	—	OUT	A1	Address bus
A0	TTL OUT	—	OUT	A0	Address bus
PA7/SCLK1	CMOS-IN PULL-UP	—	Not used		
PA6/CTS1	CMOS-IN PULL-UP	↑	IN	LCTS-0	L-CPU CTS signal
PA5/RXD1	CMOS-IN PULL-UP	↑	IN	LRXD-1	L-CPU⇒M-CPU serial I/F receive data
PA4/TXD1	CMOS-IN PULL-UP	—	OUT	LTXD-0	M-CPU⇒L-CPU serial I/F send data
PA3/SCLK0	CMOS-IN PULL-UP	—	OUT	MREQP-0	M-CPU⇒PFC transmission request signal
PA2/CTS0	CMOS-IN PULL-UP	—	OUT	MACKP-0	M-CPU⇒PFC reception enable signal
PA1/RXD0	CMOS-IN PULL-UP	↑	IN	PFRXD-1	PFC⇒M-CPU serial I/F receive data
PA0/TXD0	CMOS-IN PULL-UP	—	OUT	PFTXD-0	M-CPU⇒PFC serial I/F send data
PB7/TOB	CMOS-IN PULL-UP	—	OUT	RSTSW-0	Main switch OFF at L, (S42)
PB6/TOA	CMOS-IN PULL-UP	—	OUT	DRCLK-1	Drum motor reference clock, (DRM-MOT:M12)
PB5/TIB/INT7	CMOS-IN PULL-UP	—	IN	STINT-1	SYSTEM⇔MAIN transmission interrupt (STINT)
PB4/TIA/INT6	CMOS-IN PULL-UP	—	Not used		
PB3/TO9	CMOS-IN PULL-UP	—	OUT	DRMON-0	DRM-MOT ON Signal,L:ON, H:OFF (DC brushless motor), (M12)
PB2/TO8	CMOS-IN PULL-UP	—	OUT	DRMBK-0	DRM-MOT BRK signal,L:Brake, H:OFF (DC brushless motor), (M12)
PB1/TI9/INT5	CMOS-IN PULL-UP	↑	IN	PDWN-1	When 5V drops to 0V: H, Otherwise: L, Rising edge detection
PB0/TI8/INT4	CMOS-IN PULL-UP	—	IN	EINT0-1	External I/F input 1 (image quality control)

Port Name	At reset	R	IN/OUT	Signal Name	FUNCTION
PC7/AN7	CMOS-IN	—	IN	FUSSW-1	Fuser unit, L: Uninstalled, H: Installed
PC6/AN6	CMOS-IN	—	IN	STHU-1A	Upper heatroller thermistor (END), (THMSH/U)
PC5/AN5	CMOS-IN	—	IN	THML-1A	Lower heatroller thermistor (THMSH/L)
PC4/AN4	CMOS-IN	—	IN	THMU-1A	Upper heatroller thermistor (Center), (THMSH/U)
PC3/AN3	CMOS-IN	—	IN	CTDS-1	Image density sensor Analog input, (IQM)
PC2/AN2	CMOS-IN	—	IN	DRTMP-1	Drum thermistor analog input, (THMSD)
PC1/AN1	CMOS-IN	—	IN	ATS-1	Auto toner sensor analog input, (ATS)
PC0/AN0	CMOS-IN	—	Not used	GND	
PD0/INT8	CMOS-IN PULL-UP	↑	IN	RXINT-1	MAIN⇔PC communications interrupt
PD4	CMOS-IN PULL-UP	—	OUT	HVTM-0	Main charger, L:ON, H:OFF, (HVT-TM)
PD3	CMOS-IN PULL-UP	—	OUT	HVTT-0	Transfer belt bias, L:ON, H:OFF, (HVT-TM)
PD2	CMOS-IN PULL-UP	—	OUT	HVDDC-0	Developer bias (DC),L:ON, H:OFF,(HVT-DB)
PD1	CMOS-IN PULL-UP	↑	IN	PFACK-1	PFC→M-CPU transmission enable signal
PE7	CMOS-IN PULL-UP	—	OUT	HVDAC-0	Developer bias (AC),L:ON, H:OFF,(HVT-DB)
PE6	CMOS-IN PULL-UP	—	OUT	LRTS-0	M-CPU→L-CPU transmission request signal (enable:L)
PE5	CMOS-IN PULL-UP	—	OUT	HVTBB-0	Transfer belt brush bias , L:ON, H:OFF, (HVT-TM)
PE4	CMOS-IN PULL-UP	X	IN	IPCSW-1	Finisher PC board, L:connected, H:disconnected
PE3	CMOS-IN PULL-UP	—	OUT	DRMCW-0	Drum motor rotation direction, H:CCW, L:CW, (DC brushless motor), (DRM-MOT:M12)
PE2	CMOS-IN PULL-UP	—	OUT	LRST-0	L-CPU reset signal, L: Reset, H: Normal
PE1	CMOS-IN PULL-UP	—	OUT	FNOF2-0	Fan speed signal-2, L: Low speed, H: High speed
PE0	CMOS-IN PULL-UP	—	OUT	FANOF-0	Fan speed signal-1, L: Low speed, H: High speed
DAREFH		—	—	5V	Reference voltage of D/A convertor
DAREFL		—	—	GND	
DAOUT0		—	Not used		
DAOUT1		—	Not used		
NMI	CMOS-IN	—	IN	5V	Non Maskable Interrupt
EA	CMOS-IN	—	IN	GND	External Access
CLR	CMOS-IN	—	IN	RST-0	Reset at L
CLK	TTL-OUT	—	OUT		Clock
WDOUT	TTL-OUT	—	OUT	WDT-0	Microcontroller out of control: L, Normal: H

Port Name	At reset	R	IN/OUT	Signal Name	FUNCTION
AM8/16		—	—	GND	Bus width, Mixed 8- and 16-bit buses at L
RESET		—	—		Reset signal
VREFH		—	IN		Reference voltage input for A/D converter
VREFL		—	IN		Reference voltage input for A/D converter
AVCC		—	—		A/D converter power supply
AVSS		—			A/D converter power supply
X1/X2		—			Oscillator terminal
DVCC		—			5V power supply
DVSS		—			GND terminal

R : Programmable pull-up resistor
↑ : Pulled up
X : Not pulled up
— : No pull-up functions

1.1.2 PFC-CPU (TMP91C640N)

(1) Features

This 8-bit CMOS microcontroller integrates an 8-bit CPU, ROM, RAM, A/D converter, multifunction timer/event counter, and general-use serial interface in a single chip. External memory can be expanded to 48 Kbytes for proglam, and data memory to 1 Mbytes.

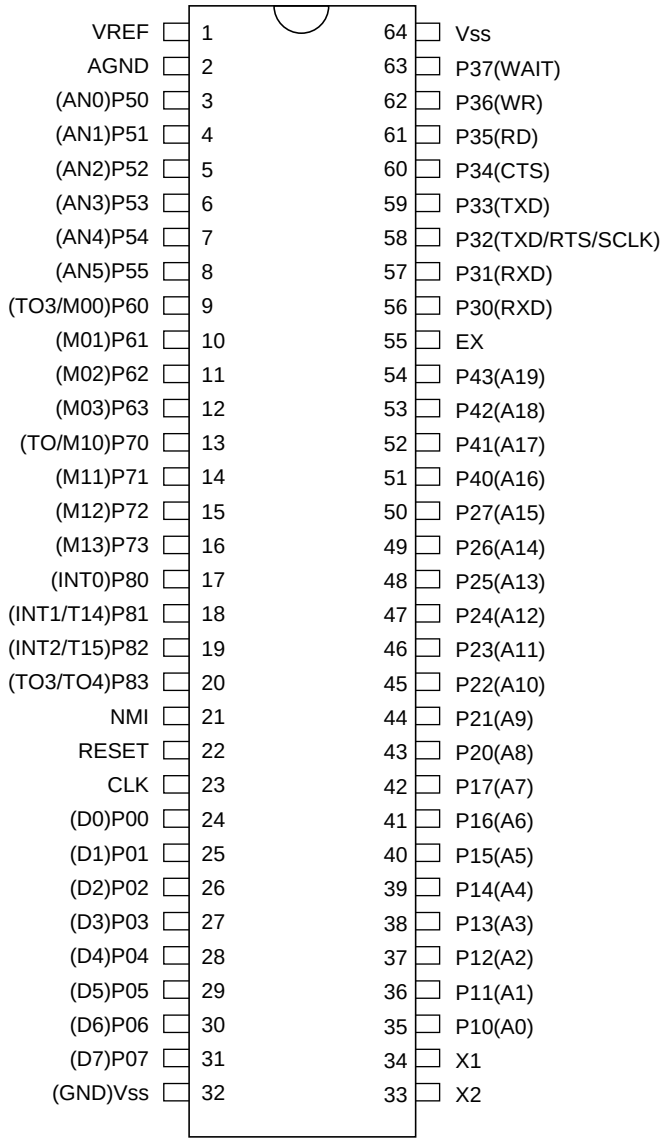
- Internal ROM: 16 Kbytes
- Internal RAM: 512 bytes
- External program memory: 48 Kbytes
- External data memory: 1 Mbytes
- Precision 8-bit A/D converter (6 ch)
- General-use serial interface (1 ch)
- Stepping motor control (2 ch)
- 54 I/O port terminals

(2) PFC-CPU functions

PFC controls the paper feed system.

All operations for transporting the paper feeding from each cassette up to the aligning rollers in the machine are controlled by PFC.

(3) Pin assignment of PFC-CPU



TMP91C640N pin assignment (shrink DIP)

I/O Map of PFC-CPU

Port Name	At reset	IN/OUT	Signal Name	FUNCTION
P37/WAIT		Not used		
P36/WR		Not used		
P35/RD		OUT	PFREQ-1	Send request (TO G/A)
P34/CTS		IN	MACKP-1	ACK signal (FROM G/A)
P33/TXD		OUT	PFRXD-0	Serial transmission data (TO G/A)
P32/TXD/RTS/ SCLK		OUT	PFACK-1	ACK signal (TO G/A)
P31/RXD		IN	PFTXD-0	Serial receive data (FROM G/A)
P30/RXD		IN	PSTPC-1	Paper stop switch (P-STP-SW:S13) When paper is past: H, No paper: L
P55/AN5		IN	24VCK-1	Front door check (analog voltage) Front door open at 2.5 V or less
P54/AN4		IN	ADCNT-1	ADU connection status When installed: L
P53/AN3		IN	5VSW-1	
P52/AN2		Not used		
P51/AN1		Not used		
P50/AN0		Not used		
P83/TO3/TO4		OUT	PSTPD-0	Paper feed status signal
P82/INT2/TI5		Not used		
P81/INT1/TI4		IN	MREQP-1	Send request (from G/A): External interrupt
P80/INT0		IN	RSTRT-1	Copier aligning roller restart signal
P73/M13		OUT	SIDMD-0	ADU Side guide motor control signal (SID-MOT:M9)
P72/M12		OUT	SIDMC-0	
P71/M11		OUT	SIDMB-0	
P70/M10/TO2		OUT	SIDMA-0	
P63/M03		OUT	ENDMD-0	ADU End guide motor control signal (END-MOT:M8)
P62/M02		OUT	ENDMC-0	
P61/M01		OUT	ENDMB-0	
P60/M00/TO1		OUT	ENDMA-0	
P07/D7		OUT	DRV7-1	Driver control signal
P06/D6		OUT	DRV6-1	
P05/D5		OUT	DRV5-1	
P04/D4		OUT	DRV4-1	
P03/D3		OUT	DRV3-1	
P02/D2		OUT	DRV2-1	
P01/D1		OUT	DRV1-1	
P00/D0		OUT	DRV0-1	

Port Name	At reset	IN/OUT	Signal Name	FUNCTION
P43/A19		OUT	CLKD-0	For driver control data (DRV0 to 7)
P42/A18		OUT	CLKC-0	Registration control signal
P41/A17		OUT	CLKB-0	Registration data output: rising edge
P40/A16		OUT	CLKA-0	Registration output data for holding: falling edge
P27/A15		Not used		
P26/A14		Not used		
P25/A13		OUT	SCSWF-0	Enable signal for bus buffer
P24/A12		OUT	SCSWE-0	
P23/A11		OUT	SCSWD-0	
P22/A10		OUT	SCSWC-0	
P21/A9		OUT	SCSWB-0	
P20/A8		OUT	SCSWA-0	
P17/A7		IN	RETS7-1	Switch, sensor input (bus buffer)
P16/A6		IN	RETS6-1	
P15/A5		IN	RETS5-1	
P14/A4		IN	RETS4-1	
P13/A3		IN	RETS3-1	
P12/A2		IN	RETS2-1	
P11/A1		IN	RETS1-1	
P10/A0		IN	RETS0-1	
NMI		IN	5V	Non mastkable Interrupt
EA		IN	GND	External access
RST		IN	PFRST-0	Reset signal
CK		Not used		
X1		IN		Oscillator input
X2		IN		Oscillator output
VREF		—		Reference voltage input for A/D converter
AGND		—		Ground input for A/D converter

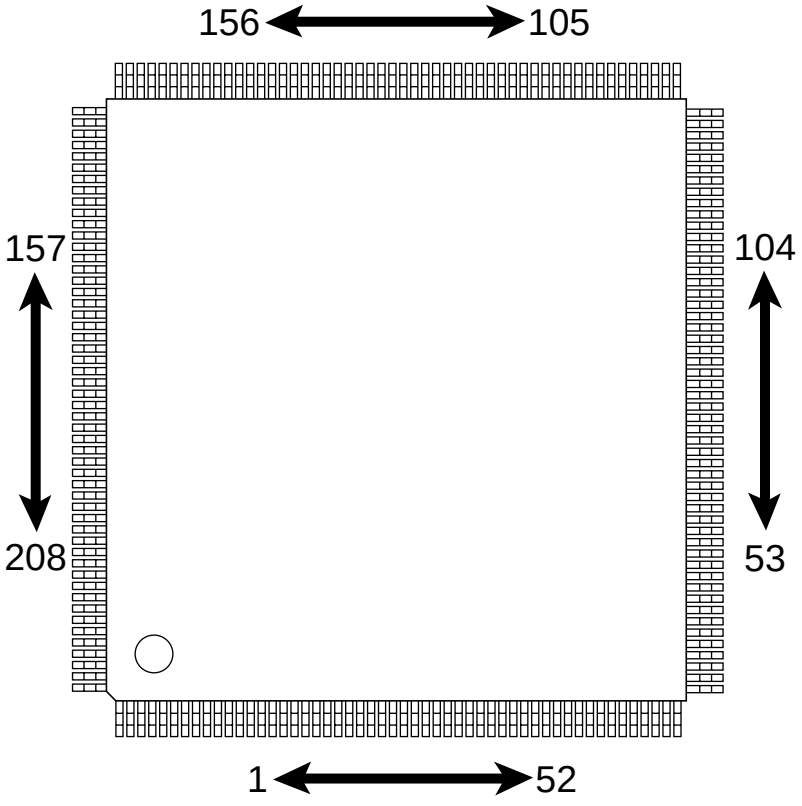
1.1.3 Gate Array (LCA301)

(1) Gate array functions

The gate array is controlled by the main CPU and the gate array's internal logic circuit. The gate array has the following functions:

- Pulse motor control (drum, transfer belt)
- Interface with NV-RAM (A key circuit is provided to prevent against clearing data inadvertently even if the microcontroller is out of control).
- General-use I/O port

(2) Gate array pin assignment diagram



I/O Map of Gate Array

Port Name	At reset	IN/OUT	Signal Name	FUNCTION
PA0	CMOS-IN	IN	CNT-1	Line jumper wire L: Line for factory adjustment), H: Field (for delivery)
PA1	CMOS-IN	IN	PCCNT-0A	PC connection line
PA2	CMOS-IN	IN	PCDSR-0	DSR signal for PC
PA3	CMOS-IN	IN	CPMSW-0	
PA4	CMOS-IN	IN	CPSW2-0	
PA5	CMOS-IN	IN	Not used	
PA6	CMOS-IN	IN	Not used	
PA7	CMOS-IN	IN	Not used	
PB0	CMOS-IN	OUT	RMS0-1	RMS
PB1	CMOS-IN	OUT	RMS1-1	
PB2	CMOS-IN	OUT	RMS2-1	
PB3	CMOS-IN	OUT	RMS3-1	
PB4	CMOS-IN	OUT	RMS4-1	
PB5	CMOS-IN	OUT	RMS5-1	
PB6	CMOS-IN	OUT	RMS6-1	
PB7	CMOS-IN	OUT	RMS7-1	
PC0	CMOS-OUT H	OUT	Not used	
PC1	CMOS-OUT H	OUT	Not used	
PC2	CMOS-OUT H	OUT	Not used	
PC3	CMOS-OUT H	OUT	Not used	
PC4	CMOS-OUT H	OUT	Not used	
PC5	CMOS-OUT H	OUT	Not used	
PC6	CMOS-OUT H	OUT	Not used	
PC7	CMOS-OUT H	OUT	Not used	
A0	TTL-IN PULL-UP	IN	A0	Address bus
A1	TTL-IN PULL-UP	IN	A1	
A2	TTL-IN PULL-UP	IN	A2	
A3	TTL-IN PULL-UP	IN	A3	
A4	TTL-IN PULL-UP	IN	A4	
A5	TTL-IN PULL-UP	IN	A5	
A6	TTL-IN PULL-UP	IN	A6	
A7	TTL-IN PULL-UP	IN	A7	
A12	TTL-IN PULL-UP	IN	A12	
A13	TTL-IN PULL-UP	IN	A13	
A14	TTL-IN PULL-UP	IN	A14	
D0	TTL-IN CMOS-OUT PULL-UP	IN/OUT	D0	Data bus

Port Name	At reset	IN/OUT	Signal Name	FUNCTION
D1	TTL-IN CMOS-OUT PULL-UP	IN/OUT	D1	Data bus
D2	TTL-IN CMOS-OUT PULL-UP	IN/OUT	D2	
D3	TTL-IN CMOS-OUT PULL-UP	IN/OUT	D3	
D4	TTL-IN CMOS-OUT PULL-UP	IN/OUT	D4	
D5	TTL-IN CMOS-OUT PULL-UP	IN/OUT	D5	
D6	TTL-IN CMOS-OUT PULL-UP	IN/OUT	D6	
D7	TTL-IN CMOS-OUT PULL-UP	IN/OUT	D7	
RD	TTL-IN PULL-UP	IN	RD-0	Read signal
WR	TTL-IN PULL-UP	IN	WR-0	Write signal
CS	TTL-IN PULL-UP	IN	CS0-0	Chip select signal
CTS	TTL-IN	IN	PCCTS-0	CTS signal for PC
RXD	TTL-IN	IN	PCRXD-0	PC serial receive data (from PC)
CBSY	TTL-IN	IN	CBSY-0	System I/F command BSY signal
CMD	TTL-IN	IN	CMD-0	System I/F receive data signal
SACK	TTL-IN	IN	SACK-0	System I/F status ACK signal
SERR	TTL-IN	IN	SERR-0	System I/F status error signal
RXDINT	CMOS-OUT H	OUT	RXINT-1	MAIN⇔PC reception interrupt (RXINT)
TXDINT	CMOS-OUT H	OUT	TXINT-1	MAIN⇔PC transmission interrupt (TXINT)
CMDINT	CMOS-OUT H	OUT	CMINT-1	System I/F reception interrupt
STSINT	CMOS-OUT H	OUT	STINT-1	System I/F transmission interrupt
RTS	CMOS-OUT H	OUT	PCRTS-0	For external PC
TXD	CMOS-OUT H	OUT	PCTXD-0	PC serial data send data (to PC)
SBSY	CMOS-OUT H	OUT	SBSY-0	System I/F status BSY signal
STS	CMOS-OUT H	OUT	STS-0	System I/F send data signal
CACK	CMOS-OUT H	OUT	CACK-0	System I/F command ACK signal
CERR	CMOS-OUT H	OUT	CERR-0	System I/F command error signal
SCLK	CMOS-IN	IN	Not used	
RESET	CMOS-IN SCHMITT	IN	GARST-0	Reset signal
CNTRST	CMOS-IN	IN	Not used	H
TESTSW	CMOS-IN	IN	Not used	GND
TSTEN	INPUT with PULL-DOWN	IN	Not used	GND
PD0	CMOS-OUT H	OUT	STKSL-0	Gate solenoid, L:ON, H:OFF, (GATE-SOL:SOL4)
PD1	CMOS-OUT H	Not used		
PD2	CMOS-OUT H	OUT	CLMTA-0	Main charger cleaning motor (CLN-MOT:M11)
PD3	CMOS-OUT H	OUT	CLMTB-0	

PD2	PD3	
H	H	Brake
H	L	CW
L	H	CCW
L	L	OFF

Port Name	At reset	IN/OUT	Signal Name	FUNCTION
PD4	CMOS-OUT H	OUT	FURMT-0	Fur brush motor, L: ON, H: OFF, (FUR-MOT:M10)
PD5	CMOS-OUT H	Not used		
PD6	CMOS-OUT H	OUT	CTRON-0	ON at counter:L, OFF at counter: H, (T)
PD7	CMOS-OUT H	Not used		
PE0	CMOS-OUT H	Not used		
PE1	CMOS-OUT H	Not used		
PE2	CMOS-OUT H	Not used		
PE3	CMOS-OUT H	Not used		
PE4	CMOS-OUT H	Not used		
PE5	CMOS-OUT H	Not used		
PE6	CMOS-OUT H	Not used		
PE7	CMOS-OUT H	Not used		
OSC1	IN	IN	X1	Oscillator input
OSC2	OUT	OUT	X2	Oscillator output
DICH1	CMOS-OUT L	OUT	DADAT-1	D/A serial data
LDCH1	CMOS-OUT L	OUT	DALTH-1	D/A serial data strobe, L: Latch, H: Hold
CLKCH1	CMOS-OUT L	OUT	SCK-1	D/A serial clock
DICH2	CMOS-OUT L	Not used		
LDCH2	CMOS-OUT L	Not used		
CLKCH2	CMOS-OUT L	Not used		
PF0	CMOS-OUT IN	IN	EXCSW-1A	Reverse door switch, H:CLOSE, L:OPEN, (EXC-SW:S19)
PF1	CMOS-OUT IN	IN	MCLSW-0	Main charger cleaning switch ON:L, OFF:H, (CLN-M-SW:S16)
PF2	CMOS-OUT IN	IN	CLNSW-0	Cleaner connection signal, L: Connection, H: No connection
PF3	CMOS-OUT IN	IN	BRMRK-1A	Brush motor lock detection signal, L: Normal, H: Lock
PF4	CMOS-OUT IN	IN	ATSSW-1	Auto toner sensor connection signal, L: Connection, H: No connection
PF5	CMOS-OUT IN	IN	CTRCN-1A	Total counter connection signal, L: Connection, H: No connection
PF6	CMOS-OUT IN	IN	EXPON-0	Exposure lamp ON signal, H: ON, L: OFF
PF7	CMOS-OUT IN	Not used		
PG0	CMOS-OUT H	OUT	USSR-1	SSR for heater lamp, L:ON. H:OFF, (SSR-U)
PG1	CMOS-OUT H	OUT	SBSSR-0	SSR for sub heater lamp, L:ON. H:OFF, (SSR-S)
PG2	CMOS-OUT H	OUT	HTRMT-1	Heat roller motor, L:ON, H:OFF,(HTR-MOT:M18)

Port Name	At reset	IN/OUT	Signal Name	FUNCTION
PG3	CMOS-OUT H	OUT	HTRML-0	Heat roller motor, L:Low speed ON, H:OFF,(HTR-MOT:M18)
PG4	CMOS-OUT H	OUT	SCRP-0	Scraper solenoid, L:ON, H:OFF,(SCRP-SOL:SOL3)
PG5	CMOS-OUT H	OUT	RVSF-0	Reverse fan motor, L:ON, H:OFF, (REV-FAN-MOT:M27)
PG6	CMOS-OUT H	OUT	DCTOF-0	Duct out fan motor, L:ON, H:OFF, (DUCT-OUT-FAN-MOT:M23)
PG7	CMOS-OUT H	OUT	HTRFA-0	Heater fan motor, L:ON, H:OFF, (HTR-FAN-MOT:M20)
PH0	CMOS-OUT H	OUT	EXTFA-0	Exit fan motor, L:ON, H:OFF, (EXIT-FAN-MOT:M19)
PH1	CMOS-OUT H	OUT	DEVFA-0	Main charger fan motor, L:ON, H:OFF, (DEV-FAN-MOT:M21)
PH2	CMOS-OUT H	OUT	CHFAN-0	Main charger fan motor, L:ON, H:OFF, (DEV-FAN-MOT:M21)
PH3	CMOS-OUT H	OUT	DCTIF-0	Duct in fan motor, L:ON, H:OFF, (DUCT-IN-FAN-MOT:M22)
PH4	CMOS-OUT H	OUT	TNRMT-0	Toner motor, L:ON, H:OFF, (TNR-MOT:M14)
PH5	CMOS-OUT H	OUT	DEVON-0	Developer motor, L:ON, H:OFF, (DEV-MOT:M16)
PH6	CMOS-OUT H	OUT	DVMBK-0	Developer motor, L:BRAKE, H:NORMAL, (DEV-MOT:M16)
PH7	CMOS-OUT H	OUT	DRMSW-0	Drum motor drive current select, L:Acceleration, H:Constant, (DRM-MOT:M12)
P10	CMOS-IN	IN	TEMP-0A	Toner Empty:L, Normal:H(TNR-EMP-SW:S14)
P11	CMOS-N	IN	HOPSW-1	Toner supply cover switch, H:open, L:close (TNR-HOP-SW:S11)
P12	CMOS-IN	IN	KCTRC-1A	Key counter connecting signal L;connect, H:disconnect
P13	CMOS-N	IN	HTRDY-1	At HTR-ready :L, other:H
P14	CMOS-IN	Not used		
P15	CMOS-IN	Not used		
P16	CMOS-IN	Not used		
P17	CMOS-IN	Not used		
DCCLK1	CMOS-OUT H	OUT	ADDCK-1	ADU-MOT reference clock, (M24)
DCCLK2	CMOS-OUT H	OUT	HTRCK-1	HTR-MOT reference clock, (M18)
DCCLK3	CMOS-OUT H	OUT	DEVCK-1	DEV-MOT reference clock, (M16)
DCCLK4	CMOS-OUT H	OUT	PFMCK-1	PFP-MOT reference clock (M31)

Port Name	At reset	IN/OUT	Signal Name	FUNCTION
SM_A	CMOS-OUT H	OUT	DRMTA-0	Drum motor control signal (Active low), (M12)
SM_B	CMOS-OUT H	OUT	DRMTB-0	
SM_NA	CMOS-OUT H	OUT	DRMTC-0	
SM_NB	CMOS-OUT H	OUT	DRMTD-0	
SMCLK	CMOS-IN	IN	DRCLK-1	Drum motor reference clock (fromM-CPU)
PJ0	CMOS-OUT H	OUT	TCMTB-0	Transfer belt cam motor (TRB-CAM-MOT:M26)
PJ1	CMOS-OUT H	OUT	TCMTA-0	
PJ2	CMOS-OUT H	OUT	AUGMT-0	Toner transport motor, L:ON, H:OFF, (AUG2-MOT:M15)
PJ3	CMOS-OUT H	OUT	RSTRT-1	RESTART (⇒PFC)
PJ4	CMOS-OUT H	OUT	PCDTR-0	For external PC
PJ5	CMOS-OUT H	Not used		
PJ6	CMOS-OUT H	Not used		
PJ7	CMOS-OUT H	Not used		
MWR	CMOS-OUT H	OUT	WRRAM-0	RAM write signal
SMINT	CMOS-OUT H	Not used		
CS0	CMOS-OUT H	Not used		
CS1	CMOS-OUT H	OUT	CSRAM-0	RAM chip select signal (8KB)
CS2	CMOS-OUT H	Not used		
CS3	CMOS-OUT H	Not used		
CS4	CMOS-OUT H	Not used		
CS5	CMOS-OUT H	Not used		
PK0	CMOS-IN	IN	TRCS1-0	Transfer belt separation switch (TR-SEP-SW:S44)
PK1	CMOS-IN	IN	TRCS-0	Transfer belt touch switch(TR-TCH-SW:S43)
PK2	CMOS-IN	IN	AGMRK-1A	Toner transport motor Lock signal L:NORMAL, H:LOCK, (AUG2-MOT:M15)
PK3	CMOS-IN	IN	PSTPC-1	Paper stop switch, L: No paper, H: When paper is past, (PSTP-SW:S13)
PK4	CMOS-IN	IN	PSTPD-0	Paper feed status signal
PK5	CMOS-IN	Not used		
PK6	CMOS-IN	Not used		
PK7	CMOS-IN	Not used		
MULTD0	CMOS-IN	Not used		

PJ0	PJ1	
H	H	Brake
L	H	CW
H	L	CCW
L	L	STOP

Port Name	At reset	IN/OUT	Signal Name	FUNCTION
MULTD1	CMOS-IN	IN	REVCL-0	Reverse clutch signal, (REV-CLT:CL2)
MULTA	CMOS-IN	IN	STKCL-0	Stack clutch control signal, (STK-
MULTY	CMOS-OUT H	OUT	REVCL-0A	CLT:CL3)
				Reverse clutch signal, L;ON, H:OFF, (REV-CLT:CL2)

1.1.4 Scanner CPU (TMP95C063F)

(1) Outline and Features

The same TMP95C063F as the main CPU is used for the scanner CPU. For details, refer to the item for the main CPU.

(2) Scanner CPU functions

The scanner CPU has respective interface with the system CPU and the ADF, and controls scanner operations.

It is also in charge of setting the various ASIC (SIPS, SH) parameters for image processing (pre-processing).

(3) Pin assignments of scanner CPU: See the item for the main CPU.

Scanner CPU I/O map

S/N	PIN	Port Name	R	IN/OUT	Signal Name	FUNCTION	
1	117	A0	—	OUT	CPUA0	Address bus	—
2	116	A1	—	OUT	CPUA1	Address bus	—
3	115	A2	—	OUT	CPUA2	Address bus	—
4	114	A3	—	OUT	CPUA3	Address bus	—
5	113	A4	—	OUT	CPUA4	Address bus	—
6	112	A5	—	OUT	CPUA5	Address bus	—
7	111	A6	—	OUT	CPUA6	Address bus	—
8	110	A7	—	OUT	CPUA7	Address bus	—
9	109	A8	—	OUT	CPUA8	Address bus	—
10	107	A9	—	OUT	CPUA9	Address bus	—
11	106	A10	—	OUT	CPUA10	Address bus	—
12	105	A11	—	OUT	CPUA11	Address bus	—
13	104	A12	—	OUT	CPUA12	Address bus	—
14	103	A13	—	OUT	CPUA13	Address bus	—
15	102	A14	—	OUT	CPUA14	Address bus	—
16	101	A15	—	OUT	CPUA15	Address bus	—
17	35	AM8/16	—	IN	SG	Bus width selection	(mixed 8- and 16-bit buses)
18	144	AVCC	—	—	+5V	A/D converter power supply	(fixed to 5V)
19	143	AVSS	—	—	SG	A/D converter ground	(fixed to ground)
20	36	CLK	—	—	(OPEN)	Not used	—
21	75	D0	—	IN/OUT	CPUD0	Data bus	—
22	76	D1	—	IN/OUT	CPUD1	Data bus	—
23	77	D2	—	IN/OUT	CPUD2	Data bus	—
24	78	D3	—	IN/OUT	CPUD3	Data bus	—
25	79	D4	—	IN/OUT	CPUD4	Data bus	—
26	80	D5	—	IN/OUT	CPUD5	Data bus	—
27	81	D6	—	IN/OUT	CPUD6	Data bus	—
28	82	D7	—	IN/OUT	CPUD7	Data bus	—

S/N	PIN	Port Name	R	IN/OUT	Signal Name	FUNCTION	
29	84	D8	—	IN/OUT	CPUD8	Data bus	—
30	85	D9	—	IN/OUT	CPUD9	Data bus	—
31	86	D10	—	IN/OUT	CPUD10	Data bus	—
32	87	D11	—	IN/OUT	CPUD11	Data bus	—
33	88	D12	—	IN/OUT	CPUD12	Data bus	—
34	89	D13	—	IN/OUT	CPUD13	Data bus	—
35	90	D14	—	IN/OUT	CPUD14	Data bus	—
36	91	D15	—	IN/OUT	CPUD15	Data bus	—
37	3	DAOUT0	—	OUT	SCNLIM	Scanner motor driving current setting (Vref)	Increasing this setting increases the current
38	4	DAOUT1	—	—	(OPEN)	Not used	—
39	1	DAREFH	—	IN	+5V	Reference voltage terminal (upper limit) for D/A converter	— —
40	2	DAREFL	—	IN	SG	Reference voltage terminal (lower limit) for D/A converter	—
41	18	DVCC	—	—	+5V	5V power supply	
42	48	DVCC	—	—	+5V	5V power supply	—
43	84	DVCC	—	—	+5V	5V power supply	—
44	108	DVCC	—	—	+5V	5V power supply	—
45	132	DVCC	—	—	+5V	5V power supply	—
46	5	DVSS	—	—	SG	GND terminal	—
47	37	DVSS	—	—	SG	GND terminal	—
48	57	DVSS	—	—	SG	GND terminal	—
49	74	DVSS	—	—	SG	GND terminal	—
50	92	DVSS	—	—	SG	GND terminal	—
51	118	DVSS	—	—	SG	GND terminal	—
52	40	EA	—	IN	SG	(external access)	(internal ROM)
53	23	NMI	—	IN	+5V	Not used	Fixed: H
54	100	A16	—	OUT	A16	Address bus	—
55	99	P21/A17	—	—	(OPEN)	Not used	—
56	98	P22/A18	—	—	(OPEN)	Not used	—
57	97	P23/A19	—	OUT	WDTEN	Watchdog enable	Enable:H, Disable:N
58	96	P24/A20	—	—	(OPEN)	Not used	—
59	95	P25/A21	—	—	(OPEN)	Not used	—
60	94	P26/A22	—	—	(OPEN)	Not used	—
61	93	P27/A23	—	—	(OPEN)	Not used	—
62	71	P52	—	OUT	JIGER	Enable jig	At completion of SLG operation: L
63	70	P53	—	OUT	JIGOK	Jig OK	At error detection: L

S/N	PIN	Port Name	R	IN/OUT	Signal Name	FUNCTION	
64	69	P54	—	—	(OPEN)	Not used	—
65	68	RW	—	OUT	CPURW	Write/Read to special register	L active
66	67	CS0	—	OUT	CPUCS0	SRAM chip select	L active
67	66	CS2	—	OUT	CPUCS2	PROM chip select	L active
68	65	CS1	—	OUT	CPUCS1	SH (CCD) chip select	L active
69	64	P61	—	OUT	VSYNC	Image vertical synchronization	—
70	63	P62	—	OUT	FAN3SP	SLG Fan speed selection (SLG-FAN-MOT:M4)	High speed: H, Low speed: L
71	62	P63	—	OUT	FAN3ON	SLG Fan ON/OFF signal (SLG-FAN-MOT:M4)	ON:L, OFF:H
72	61	CS3	—	OUT	CPUCS3	SIPS chip select	L active
73	60	P65	—	OUT	PHSCHG	SH mode switching	
74	59	P66	—	OUT	FAN2SP	OPT Fan speed selection (OPT-FAN-MOT:M3-2)	High speed: H, Low speed: L
75	58	P67	—	OUT	FAN2ON	OPT Fan ON/OFF (OPT-FAN-MOT (M3-2)	ON:L, OFF:H
76	49	PG00	—	OUT	DCM-A	DCM motor phase A (DCM-MOT:M2)	L active
77	50	PG01	—	OUT	DCM-B	DCM motor phase B (DCM-MOT:M2)	L active
78	51	PG02	—	OUT	DCM-C	DCM motor phase C (DCM-MOT:M2)	L active
79	52	PG03	—	OUT	DCM-D	DCM motor phase D (DCM-MOT:M2)	L active
80	53	P74	X	IN	APS1	APS sensor	
81	54	P75	X	IN	APS2	APS sensor	
82	55	P76	X	IN	APS3	APS sensor	
83	56	P77	—	—	(OPEN)	Not used	—
84	32	P80	—	—	(OPEN)	Not used	—
85	33	P81	X	IN	APS4	APS sensor	—
86	34	P82	X	IN	APS5	APS sensor	—
87	43	P83	X	IN	APS6	APS sensor	—
88	44	P84/INT0	X	IN	SRTS	SYS⇒SLG transmission interrupt	L active
89	45	P85/INT1	—	—	(OPEN)	Not used	—
90	46	P86/INT2	X	IN	DFRAK	ADF⇒SLG reception enable signal	L active
91	47	P87/INT3	—	—	(OPEN)	Not used	—
92	24	P90	—	OUT	SCNDIR	Scanner motor rotation direction, (SCN-MOT:M1)	

S/N	PIN	Port Name	R	IN/OUT	Signal Name	FUNCTION	
93	25	TO1	—	OUT	SCNCLK	Scanner motor CLK (SCN-MOT:M1)	
94	26	P92	—	OUT	FAN1ON	OPT Fan ON/OFF (OPT-FAN-MOT:M3-1)	ON: L, OFF: H
95	27	P93/TO3	—	OUT	FAN1SP	OPT Fan speed selection (OPT-FAN-MOT:M3-1)	High speed: H, Low speed: L
96	28	P94	—	OUT	FAN4ON	Not used	
97	29	P95	—	OUT	EXPEN	Exposure lamp output enable	Enable: L
98	30	P96	—	OUT	EXPON	Exposure lamp ON	Lamp ON: L
99	31	P97/TO7	—	OUT	EXPPWM	Exposure intensity adjustment	PWM
100	14	TXD0	—	OUT	STXD	SLG⇒SYS serial I/F send data	Serial
101	15	RXD0	X	IN	SRXD	SYS⇒SLG serial I/F receive data	Serial
102	16	CTS0	—	OUT	SCTS	SLG⇒SYS transmission interrupt	L active
103	17	PA3	—	—	(OPEN)	Not used	—
104	19	TXD1	—	OUT	DFTXD	SLG⇒ADF serial I/F send data	Serial
105	20	RXD1	X	IN	DFRXD	ADF⇒SLG serial I/F receive data	Serial
106	21	CTS1	—	OUT	DFAK	SLG⇒ADF reception enable signal	L active
107	22	PA7	—	OUT	DFRQ	SLG⇒ADF transmission request signal	L active
108	6	PB0/TI8/INT4	—	—	(OPEN)	Not used	—
109	7	INT5	↑	IN	PWDNCK	Power down check	Power off: L
110	8	PB2/TO8	—	—	(OPEN)	Not used	—
111	9	PB3/TO9	—	—	(OPEN)	Not used	—
112	10	PB4/TIA/INT6	—	OUT	DFRRQ	ADF⇒SLG reception request signal	L active
113	11	PB5/TIB/INT7	X	IN	SCHOM	Scanner motor home SW (HOME-SW:S2)	Home position: H
114	12	PB6/TOA	↑	IN	SCNT	System board connection	Connection: L
115	13	PB7/TOB	X	IN	DFCNT	ADF connection	Connection: L
116	133	PC0/AN0	—	—	SG	Not used	—
117	134	PC1/AN1	—	—	SG	Not used	—
118	135	PC2/AN2	—	—	SG	Not used	—
119	136	PC3	—	IN	EWSCNT	EWS connection	Connection: L
120	137	PC4	—	IN	PGCNT	Pattern Generator connection	Connection: L
121	138	PC5	—	—	(OPEN)	Not used	—
122	139	PC6	—	IN	DSWCNT	DIP SW board/adjustment jig connection	Connection: L

S/N	PIN	Port Name	R	IN/OUT	Signal Name	FUNCTION	
123	140	PC7	—	IN	24VCHK	24V power supply check	Power drop: L
124	131	PD0	—	OUT	SCNMD0	Scanner motor step angle setting (SCN-MOT:M1)	
125	130	PD1	—	OUT	SCNMD1		
126	129	PD2	—	OUT	SCNMD2		
127	128	PD3	—	OUT	SCNMD3		
128	127	PD4	—	OUT	SCNHLD	Scanner motor hold	
129	126	PE0	X	IN	DIPSW8	Scanner unit standalone mode	For adjustment
130	125	PE1	X	IN	DIPSW7		
131	124	PE2	X	IN	DIPSW6		
132	123	PE3	X	IN	DIPSW5		
133	122	PE4	X	IN	DIPSW4		
134	121	PE5	X	IN	DIPSW3		
135	120	PE6	X	IN	DIPSW2		
136	119	PE7	X	IN	DIPSW1		
137	73	RD	—	OUT	CPURD	Reading	Enable: L
138	41	RESET	↑	IN	CPURST	Reset	Reset: L
139	141	VREFH	—	IN	+5V	Reference voltage input for A/D converter (H)	—
140	142	VREFL	—	IN	SG	Reference voltage input for A/D converter (L)	—
141	42	WDTOUT	—	OUT	WDTOUT	Watchdog timer output	Microcontroller malfunction (out of control): L
142	72	WR	—	OUT	CPUWR	Write	Enable: L
143	38	X1	—	IN/OUT	X1	Oscillator terminal	—
144	39	X2	—	IN/OUT	X2	Oscillator terminal	—

R : Programmable pull-up resistor
↑ : Internal pull-up enabled
X : Internal pull-up disabled
— : No internal pull-up function

1.1.5 Laser CPU (TMP95C063F)

(1) Outline and features

The same TMP95C063F as the main CPU is used for the Laser CPU. For details, refer to the item for the main CPU.

(2) Laser CPU functions

The laser CPU has an interface with the main CPU, and controls the inside of the laser unit (rotation of the polygonal motor, galvanic mirror control, laser power control, etc.)

It is also in charge of setting the various ASIC (POPS) parameters for image processing (post-processing).

(3) Pin assignments of laser CPU: See the item for the main CPU.

Laser CPU I/O map

Port Name	At reset	R	IN/OUT	Signal Name	FUNCTION
P97/TO7	CMOS-IN PULL-UP	—	OUT	(FANSP-1)	Fan speed selection, L: High speed, H: Low speed, (LSU-FAN-MOT: M6)
P96/TI6	CMOS-IN PULL-UP	—	OUT	FAN-0	Fan, L: ON, H: OFF
P95/TO5	CMOS-IN PULL-UP	↑	IN	(WUL-0)	Beam sensor window upper limit
P94/TI4	CMOS-IN PULL-UP	↑	IN	(WLL-0)	Beam sensor window lower limit
P93/TO3	CMOS-IN PULL-UP	—	OUT	OFFST-0	Beam sensor detection mode, L: Detection
P92/TI2	CMOS-IN PULL-UP	—	OUT	BMSW2-1	Beam sensor select
P91/TO1	CMOS-IN PULL-UP	—	OUT	BMSW1-1	
P90/TI0	CMOS-IN PULL-UP	—	OUT	BMSW0-1	
P87/INT3	CMOS-IN PULL-UP	↑	IN	BUSY-0	Beam sensor busy (A/D conversion in progress), Interrupt at rise at end of conversion
P86/INT2	CMOS-IN PULL-UP	—	IN	PVDEN-0	Interrupt at rise at end of page, L: Print area
P85/INT1	CMOS-IN PULL-UP	X	IN	CNTRD-1	Reading from POPS possible, H: Read
P84/INT0	CMOS-IN PULL-UP	X	IN	COMINT-0	Interrupt from monitor IC, L: Buffer empty
P83/NMI2	CMOS-IN PULL-UP	—	OUT	COMND-1	Command/data select output to monitor IC
P82/WAIT	CMOS-IN PULL-UP	—	OUT	(CLKEN-1)	Crystal oscillator enable, L: Disable, H: Enable
P81/SCOUT	CMOS-IN PULL-UP	—	OUT	BUSEN-1	Bus release with POPS at EWS connection, H: Enable
P80/BS	CMOS-IN PULL-UP	—			
P77/PG13	CMOS-IN PULL-UP	↑	IN	ERR-1	HYSNC error/PWM calibration BUSY, H: Error
P76/PG12	CMOS-IN PULL-UP	—	OUT	LVDEN-0	L-CPU secondary scanning direction sync signal
P75/PG11	CMOS-IN PULL-UP	—	OUT	LE-0	Laser enable, L: Enable
P74/PG10	CMOS-IN PULL-UP	—	OUT	LDOFF-0	Forced laser OFF during manual feed, L: OFF
P73/PG03	CMOS-IN PULL-UP	—	OUT	DDISD-1	Laser driver D forced stop
P72/PG02	CMOS-IN PULL-UP	—	OUT	DDISC-1	Laser driver C forced stop
P71/PG01	CMOS-IN PULL-UP	—	OUT	DDISB-1	Laser driver B forced stop

Port Name	At reset	R	IN/OUT	Signal Name	FUNCTION
P70/PG00	CMOS-IN PULL-UP	—	OUT	DDISA-1	Laser driver A forced stop
P67/UCAS3/UW3/ WE3	TTL-OUT H	—	OUT	CNTST-0	HSYNC count of adjustment sensor, L: Count
P66/LCAS3/LW3/ REFOUT	TTL-OUT H	—	OUT	CSNVM-0	Serial EEPROM chip select, L: Select
P65/CAS3/WE3	TTL-OUT H	—	OUT	GDALAT-0	Galvanic mirror DAC latch, L: Latch
P64/CS3/RAS3	TTL-OUT H	—	OUT	CSGDAC-0	Galvanic mirror DAC chip select, L: Select
P63/UCAS1/UW1/ WE1	TTL-OUT H	—	OUT	(DAWR-0)	Beam sensor DAC latch (at compara-tor)
P62/LCAS1/LW1/ REFOUT	TTL-OUT H	—	OUT	(DASC1-0)	Beam sensor DAC select (at comparator)
P61/CAS1/WE1	TTL-OUT H	—	OUT	(DASC0-0)	
P60/CS1/RAS1	TTL-OUT H	—	OUT	CSPOPS-0	POPS chip select, L: Select
P57/CS2	TTL-OUT L	—	OUT	CSPROM-0	PROM chip select, L: Select
P56/CS0	TTL-OUT H	—	OUT	CSSRAM-0	SRAM chip select, L: Select
P55/RW	CMOS-IN PULL-UP	—	OUT	GLVMT-1	Galvanic mirror driver mute, H: Mute
P54/BUSAK	CMOS-IN PULL-UP	—	Not used		
P53/BUSRQ	CMOS-IN PULL-UP	——	Not used		
P52/HWR	CMOS-IN PULL-UP	—	Not used		
WR		—	OUT	WR-0	External memory write signal
RD		—	OUT	RD-0	External memory read signal
P27/A23	TTL-OUT H	—	OUT	LDOND-0	Laser D forced ON, L: ON, H: OFF
P26/A22	TTL-OUT H	—	OUT	LDONC-0	Laser C forced ON, L: ON, H: OFF
P25/A21	TTL-OUT H	—	OUT	LDONB-0	Laser B forced ON, L: ON, H: OFF
P24/A20	TTL-OUT H	—	OUT	LDONA-0	Laser A forced ON, L: ON, H: OFF
P23/A19	TTL-OUT H	—	OUT	LDRDY-0	Illuminating on drum inhibit signal, L: Ready, H: Copy
P22/A18	TTL-OUT H	—	OUT	SCRST-1	PWM calibration, H: Calibration
P21/A17	TTL-OUT H	—	OUT	VDIS-1	IVDEN-0 inhibit during control between pages, H: Beam control in progress
P20/A16	TTL-OUT H	—	OUT	A16	Address bus
P17/D15	TTL 3STATE	—	IN/OUT	D15	Data bus
P16/D14	TTL 3STATE	—	IN/OUT	D14	Data bus
P15/D13	TTL 3STATE	—	IN/OUT	D13	Data bus
P14/D12	TTL 3STATE	—	IN/OUT	D12	Data bus
P13/D11	TTL 3STATE	—	IN/OUT	D11	Data bus
P12/D10	TTL 3STATE	—	IN/OUT	D10	Data bus
P11/D9	TTL 3STATE	—	IN/OUT	D9	Data bus

Port Name	At reset	R	IN/OUT	Signal Name	FUNCTION
P10/D8	TTL 3STATE	—	IN/OUT	D8	Data bus
D7	TTL 3STATE	—	IN/OUT	D7	Data bus
D6	TTL 3STATE	—	IN/OUT	D6	Data bus
D5	TTL 3STATE	—	IN/OUT	D5	Data bus
D4	TTL 3STATE	—	IN/OUT	D4	Data bus
D3	TTL 3STATE	—	IN/OUT	D3	Data bus
D2	TTL 3STATE	—	IN/OUT	D2	Data bus
D1	TTL 3STATE	—	IN/OUT	D1	Data bus
D0	TTL 3STATE	—	IN/OUT	D0	Data bus
A15	TTL OUT	—	OUT	A15	Address bus
A14	TTL OUT	—	OUT	A14	Address bus
A13	TTL OUT	—	OUT	A13	Address bus
A12	TTL OUT	—	OUT	A12	Address bus
A11	TTL OUT	—	OUT	A11	Address bus
A10	TTL OUT	—	OUT	A10	Address bus
A9	TTL OUT	—	OUT	A9	Address bus
A8	TTL OUT	—	OUT	A8	Address bus
A7	TTL OUT	—	OUT	A7	Address bus
A6	TTL OUT	—	OUT	A6	Address bus
A5	TTL OUT	—	OUT	A5	Address bus
A4	TTL OUT	—	OUT	A4	Address bus
A3	TTL OUT	—	OUT	A3	Address bus
A2	TTL OUT	—	OUT	A2	Address bus
A1	TTL OUT	—	OUT	A1	Address bus
A0	TTL OUT	——	OUT	A0	Address bus
PA7/SCLK1	CMOS-IN PULL-UP	—	OUT	SCLK-1	Serial clock for laser power DAC/EEPROM
PA6/CTS1	CMOS-IN PULL-UP	—	OUT	LDDALD-0	Serial latch for laser power DAC, L: Latch
PA5/RXD1	CMOS-IN PULL-UP	↑	IN	RXD-1	Serial data for EEPROM read
PA4/TXD1	CMOS-IN PULL-UP	—	OUT	TXD-1	Serial data for laser power DAC/ EEPROM write
PA3/SCLK0	CMOS-IN PULL-UP	—	OUT	RTS-0	L-CPU⇒M-CPU send request signal
PA2/CTS0	CMOS-IN PULL-UP	↑	IN	CTS-0	M-CPU⇒L-CPU serial receive data
PA1/RXD0	CMOS-IN PULL-UP	↑	IN	RXD-0	M-CPU⇒L-CPU serial receive data
PA0/TXD0	CMOS-IN PULL-UP	—	OUT	TXD-0	L-CPU⇒M-CPU serial send data
PB7/TOB	CMOS-IN PULL-UP	—	OUT	LSBSY-0	Laser write system bus busy, L: Ready
PB6/TOA	CMOS-IN PULL-UP	—	OUT	WDEN-0	Watchdog enable, L: Enable
PB5/TIB/INT7	CMOS-IN PULL-UP	X	IN	PMOK-0	Polygonal mirror motor PLLOK, L:OK, (POL-MOT:M5)

Port Name	At reset	R	IN/OUT	Signal Name	FUNCTION
PB4/TIA/INT6	CMOS-IN PULL-UP	—	OUT	PMON-0	Polygonal mirror motor ON, L:ON
PB3/TO9	CMOS-IN PULL-UP	—	OUT	(PMBRK-0)	Polygonal mirror motor brake, L:ON
PB2/TO8	CMOS-IN PULL-UP	—	OUT	PMCLK-1	Polygonal mirror motor reference clock
PB1/TI9/INT5	CMOS-IN PULL-UP	X	IN	PDWN-1	When 5V drops to 0V: H, Otherwise: L, Rising edge detection
PB0/T18/INT4	CMOS-IN PULL-UP	↑	IN	MVDEN-0	M-CPU secondary scanning direction sync signal, L: Enable
PC7/AN7	CMOS-IN	—	IN	BMAD7-1	Beam sensor AD value (12 bits)
PC6/AN6	CMOS-IN	—	IN	BMAD6-1	
PC5/AN5	CMOS-IN	—	IN	BMAD5-1	
PC4/AN4	CMOS-IN	—	IN	BMAD4-1	
PC3/AN3	CMOS-IN	—	IN	BMAD3-1	
PC2/AN2	CMOS-IN	—	IN	BMAD2-1	
PC1/AN1	CMOS-IN	—	IN	BMAD1-1	
PC0/AN0	CMOS-IN	—	IN	BMAD0-1	
PD4	CMOS-IN PULL-UP	X	IN	EWSCN-0	Bus release at EWS connection, L: POPS⇔L-CPU release
PD3	CMOS-IN PULL-UP	↑	IN	BMAD11-1	Beam sensor AD value (12 bits)
PD2	CMOS-IN PULL-UP	↑	IN	BMAD10-1	
PD1	CMOS-IN PULL-UP	↑	IN	BMAD9-1	
PD0	CMOS-IN PULL-UP	↑	IN	BMAD8-1	
PE7	CMOS-IN PULL-UP	—	OUT	BMDA7-1	Beam sensor comparison value (at comparator)
PE6	CMOS-IN PULL-UP	—	OUT	BMDA6-1	Beam position sensor (secondary scanning direction) comparison value
PE5	CMOS-IN PULL-UP	—	OUT	BMDA5-1	Beam sensor HYSNC detection threshold value
PE4	CMOS-IN PULL-UP	—	OUT	BMDA4-1	Dual-use DA output data
PE3	CMOS-IN PULL-UP	—	OUT	BMDA3-1	
PE2	CMOS-IN PULL-UP	—	OUT	BMDA2-1	
PE1	CMOS-IN PULL-UP	—	OUT	BMDA1-1	
PE0	CMOS-IN PULL-UP	—	OUT	BMDA0-1	
DAREFH		—	—	5V	
DAREFL		—	—	GND	
DAOUT0		—	—		
DAOUT1		—	—		
NMI	CMOS-IN	—	IN	5V	
CLK	TTL-OUT	—	OUT	(SNSCK-1)	Clock to SNS

Port Name	At reset	R	IN/OUT	Signal Name	FUNCTION
WDOUT	TTL-OUT	—	OUT	WDTOUT-0	At microcontroller out of control: L, normal: H
EA		—		GND	
AM8/16		—		GND	Mixed 8- and 16-bit buses at L
RESET		—	IN	CPURST-0	Reset signal
VREFH		—	IN	5V	A/D converter reference input signal
VREFL		—	IN	GND	A/D converter reference input signal
AVCC		—		5V	A/D converter power supply
AVSS		—		GND	A/D converter power supply
X1/X2		—			Oscillator terminal
DVCC		—			5V power supply
DVSS		—			Ground terminal

R : Programmable pull-up resistor. Signals in parentheses are unused.

↑ : Pulled up

X : Not pulled up

— : No pull-up functions

1.1.6 System CPU (NR4650)

(1) Features

The NR4650 64-bit microprocessor uses MIPS's RISC architecture and features the following advanced functions.

It is also completely compatible in terms of software architecture with Integrated Device Technology's IDT79RV4650.

❍ 64-bit microprocessor with built-in advanced functions
- 64-bit integer operations
- 64-bit register
- 100 MHz, 133 MHz clock speeds

❍ High performance
- 133 MIPS (at 133 MHz clock speed)
- Integer multiplier having 66.7M Mul-Add/sec performance (at 133 MHz clock speed)
- Single-precision floating point processor of 44 MFLOP/sec (at 133 MHz clock speed)
- >300,000 dhrystone/sec (at 133 MHz clock speed) (175 dhrystone MIPS)
- Cache memory of 8 Kbytes each for instructions and data
- Integer DSP function supported
- High-speed interrupt decoding
- Cache lock function

❍ Lower power consumption
- 3.3V power voltage
- Power management function using standby mode

❍ Large internal cache memory
- Cache memory of 8 Kbytes each for instructions and data
- 2-way set-associative system
- Write back and write through supported

❍ Highly compatible with the NR3000 and NR4600 family
- Completely upwardly compatible with NR3000 and NR4600 family application software

❍ Low cost
- 32-bit bus interface mode can be set
- Low cost achieved by elimination of TLB function and double-precision floating point processor

❍ Short development provided by system support
- Extensive support for real-time operation
- Easier development of software by high compatibility with MPS III instruction sets

❍ Wide range of installable applications
- Game equipment
- Multimedia equipment
- Networking equipment
- Printers

❍ 5V interface support (only on NR4650G)
- 5V signals can be input.

(2) System CPU functions

The system CPU is used in combination with a system control LSI with dedicated PCI bridge. This CPU has interfaces with the HDD, main CPU and scanner CPU, and performs control of ASIC in the SYS board, image data processing (compression, decompression, etc.), connection processing with external network lines (LAN, DSS, etc.), and control of the control panel.

The PCI bus is released to the outside via the MTB board, and is constructed to be connectable to a LAN printer board and SCSI board.

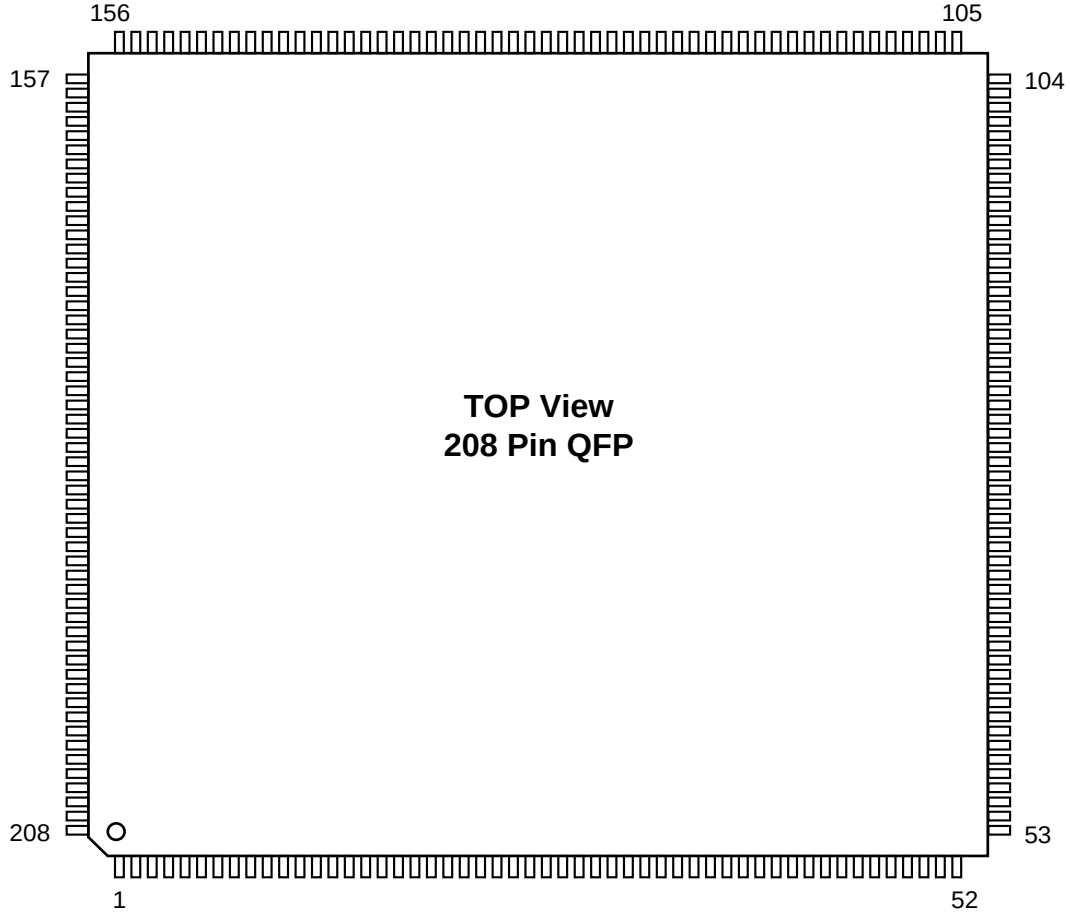
The control program is stored in external ROM (F-ROM).

The download function can be used to read new programs from a personal computer (PC).

Adjustment values for the clock and the system are stored together with setting values in battery backed up internal RAM.

(3) Pin assignment of system CPU

0.5 mm pitch 208-pin QFP type (all models)



(4) Names of Terminals and Functions

Pin No.	Function	Pin No.	Function	Pin No.	Function	Pin No.	Function
1	N.C.	53	N.C.	105	N.C.	157	N.C.
2	N.C.	54	N.C.	106	N.C.	158	N.C.
3	N.C.	55	SysCmd2	107	N.C.	159	N.C.
4	N.C.	56	SysAD36	108	N.C.	160	N.C.
5	SysAD45	57	SysAD4	109	Vcc	161	N.C.
6	SysAD13	58	SysCmd1	110	Vss	162	SysAD30
7	N.C.	59	Vss	111	SysAD21	163	Vcc
8	SysAD44	60	Vcc	112	SysAD53	164	Vss
9	Vss	61	SysAD35	113	RdRdy*	165	SysAD62
10	Vcc	62	SysAD3	114	ModeIn	166	N.C.
11	SysAD12	63	SysCmd0	115	SysAD22	167	SysAD31
12	SysCmdP	64	SysAD34	116	SysAD54	168	SysAD63
13	SysAD43	65	Vss	117	Vcc	169	Vcc
14	SysAD11	66	Vcc	118	Vss	170	Vss
15	Vss	67	N.C.	119	Release*	171	VccOK
16	Vcc	68	N.C.	120	SysAD23	172	SysADC3
17	SysCmd8	69	SysAD2	121	SysAD55	173	SysADC7
18	SysAD42	70	Int5*	122	NMI*	174	N.C.
19	SysAD10	71	SysAD33	123	Vcc	175	N.C.
20	SysCmd7	72	SysAD1	124	Vss	176	N.C.
21	Vss	73	Vss	125	SysADC2	177	N.C.
22	Vcc	74	Vcc	126	SysADC6	178	N.C.
23	SysAD41	75	Int4*	127	N.C.	179	N.C.
24	SysAD9	76	SysAD32	128	SysAD24	180	N.C.
25	SysCmd6	77	SysAD0	129	Vcc	181	VccP
26	SysAD40	78	Int3*	130	Vss	182	VssP
27	N.C.	79	Vss	131	SysAD56	183	N.C.
28	N.C.	80	Vcc	132	N.C	184	N.C.
29	Vss	81	Int2*	133	SysAD25	185	MasterClock
30	Vcc	82	SysAD16	134	SysAD57	186	N.C.
31	SysAD8	83	SysAD48	135	Vcc	187	N.C.
32	SysCmd5	84	Int1*	136	Vss	188	N.C.
33	SysADC4	85	Vss	137	N.C.	189	Vcc
34	SysADC0	86	Vcc	138	SysAD26	190	Vss
35	Vss	87	SysAD17	139	SysAD58	191	N.C.
36	Vcc	88	SysAD49	140	N.C.	192	SysADC5
37	SysACmd4	89	Int0*	141	Vcc	193	SysADC1
38	SysAD39	90	SysAD18	142	Vss	194	N.C.
39	SysAD7	91	Vss	143	SysAD27	195	Vcc
40	SysCmd3	92	Vcc	144	SysAD59	196	Vss
41	Vss	93	SysAD50	145	ColdRest*	197	SysAD47
42	Vcc	94	ValidIn*	146	SysAD28	198	SysAD15
43	SysAD38	95	SysAD19	147	Vcc	199	N.C.
44	SysAD6	96	SysAD51	148	Vss	200	SysAD46
45	ModeClock	97	Vss	149	SysAD60	201	Vcc
46	WrRdy*	98	Vcc	150	Reset*	202	Vss
47	SysAD37	99	ValidOut*	151	SysAD29	203	SysAD14
48	SysAD5	100	SysAD20	152	SysAD61	204	N.C.
49	Vss	101	SysAD52	153	N.C.	205	N.C.
50	Vcc	102	ExtRqst*	154	N.C.	206	N.C.
51	N.C.	103	N.C.	155	N.C.	207	N.C.
52	N.C.	104	N.C.	156	N.C.	208	N.X.

* N.C.: These pins are not connected as they are provided for future expandability and interchageability

(5) Description of Terminal Functions

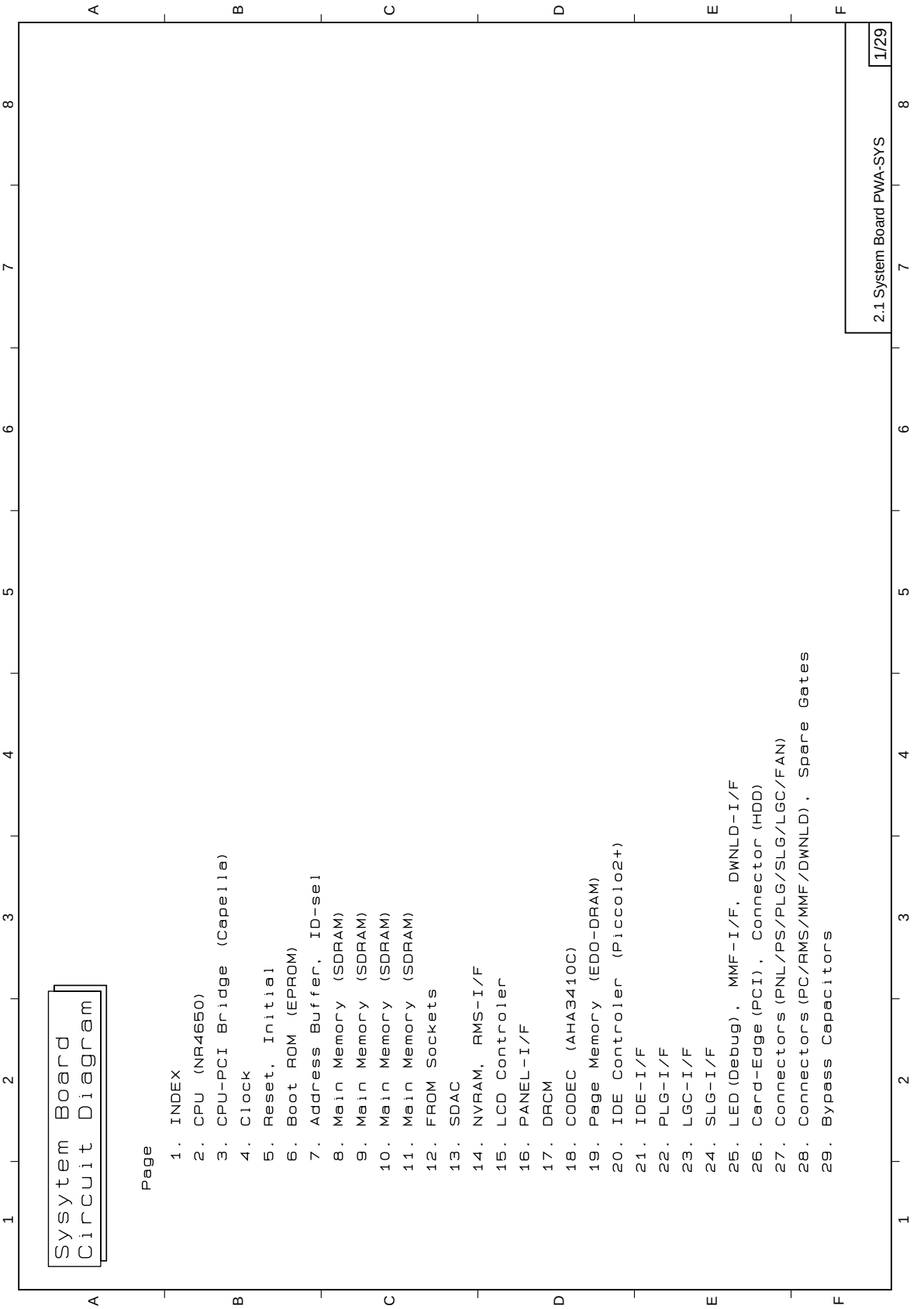
Pin Name	I/O	Description
System interface		
ExtRqst*	I	External Request: Signal by which the system interface requests issue of an external request
Release*	O	Interface release: This signal indicates that the processor has released the system interface to a slave status.
RdRdy*	I	Read Ready: This signal indicates that the external agent can accept a processor read.
WrRdy*	I	Write Ready: This signal indicates that the external agent can accept a processor write.
ValidIn*	I	Valid In: This signal indicates that the external agent is driving valid addresses or data on the SysAD bus, and valid commands or data on the SysCmd bus.
ValidOut*	O	Valid Out: This signal indicates that the processor is driving valid addresses or data on the SysAD bus, and valid commands or data on the SysCmd bus.
SysAD (63:0)	I/O	System address/data bus: This 64-bit address data bus is for communications between the processor and external agent.
SysADC (7:0)	I/O	System address/data check bus: This 8-bit bus is for the SysAD bus in the data bus cycle and contains the parity check bit.
SysCmd (8:0)	I/O	System command/data ID bus: This 9-bit bus is for communications of commands and data ID between the processor and the external agent.
SysCmdP	I/O	System command/data ID bus parity (reserved): This is “0” when at output on the NR4650, and is not used on input.
Clock/control interface		
MasterClock	I	Master clock: This is the reference clock of the system interface. The timing of all outputs are related to this clock. The pipeline operating frequency is obtained by multipling this clock.
VccP	I	Vcc for PLL: This is Vcc for internal PLL. Stable Vcc with minimum voltage fluctuations is supplied.
VssP	I	Vss for PLL: This is Vss for internal PLL. Stable Vss with minimum voltage fluctuations is supplied.

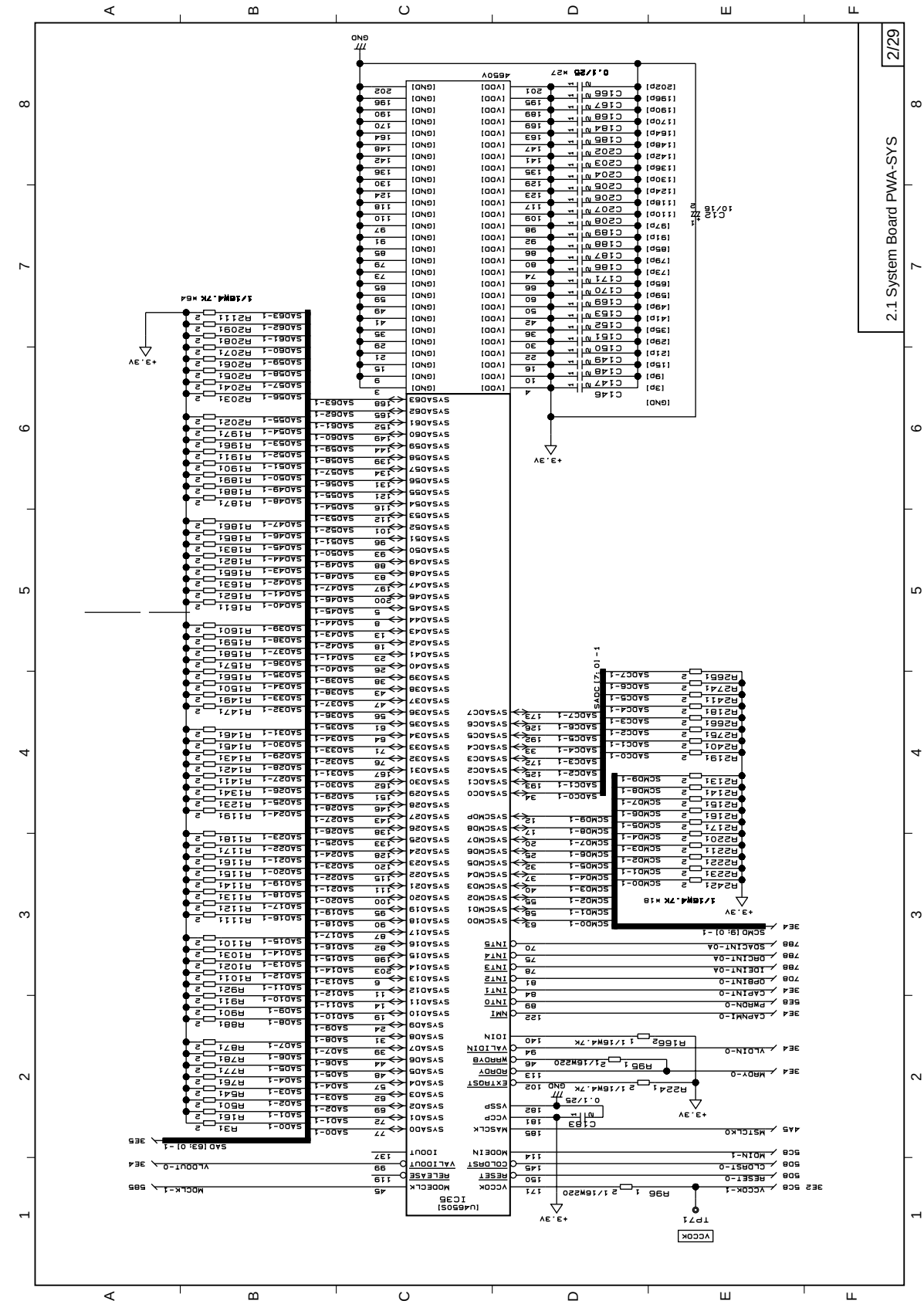
Pin Name	I/O	Description
Interrupt interface		
Int (5:0)*	I	Interrupt: Six general-purpose interrupts obtained by OR-ing bits 5:0 and each bit in the interrupt register
NMI*	I	Non-maskable interrupts: Non-maskable interrupts obtained by OR-ing the bits 6 in the interrupt register
Initialization setting interface		
VccOk	I	Vcc enable: When this signal is asserted, this indicates that the +3.3V power voltage of NR4650 is +3.0V or more for 100 msec or more, and that the status is stable. Reading of serial operation of boot time mode control is started by asserting VccOK.
ColdReset*	I	Cold Reset: This signal must be asserted by a power ON reset or cold reset. This signal must be de-asserted synchronized with the MasterClock.
Reset*	I	Reset: This signal must be asserted by all reset sequences. There is the possibility that it is synchronized or asynchronous with a cold reset, or that it is synchronized with start of a warm reset. This signal must be de-asserted synchronized with the MasterClock.
ModeClock	O	Boot mode clock: Output of the serial boot mode data clock obtained by dividing the system clock frequency by 256
ModeIn	I	Boot mode data input: Serial boot mode data input

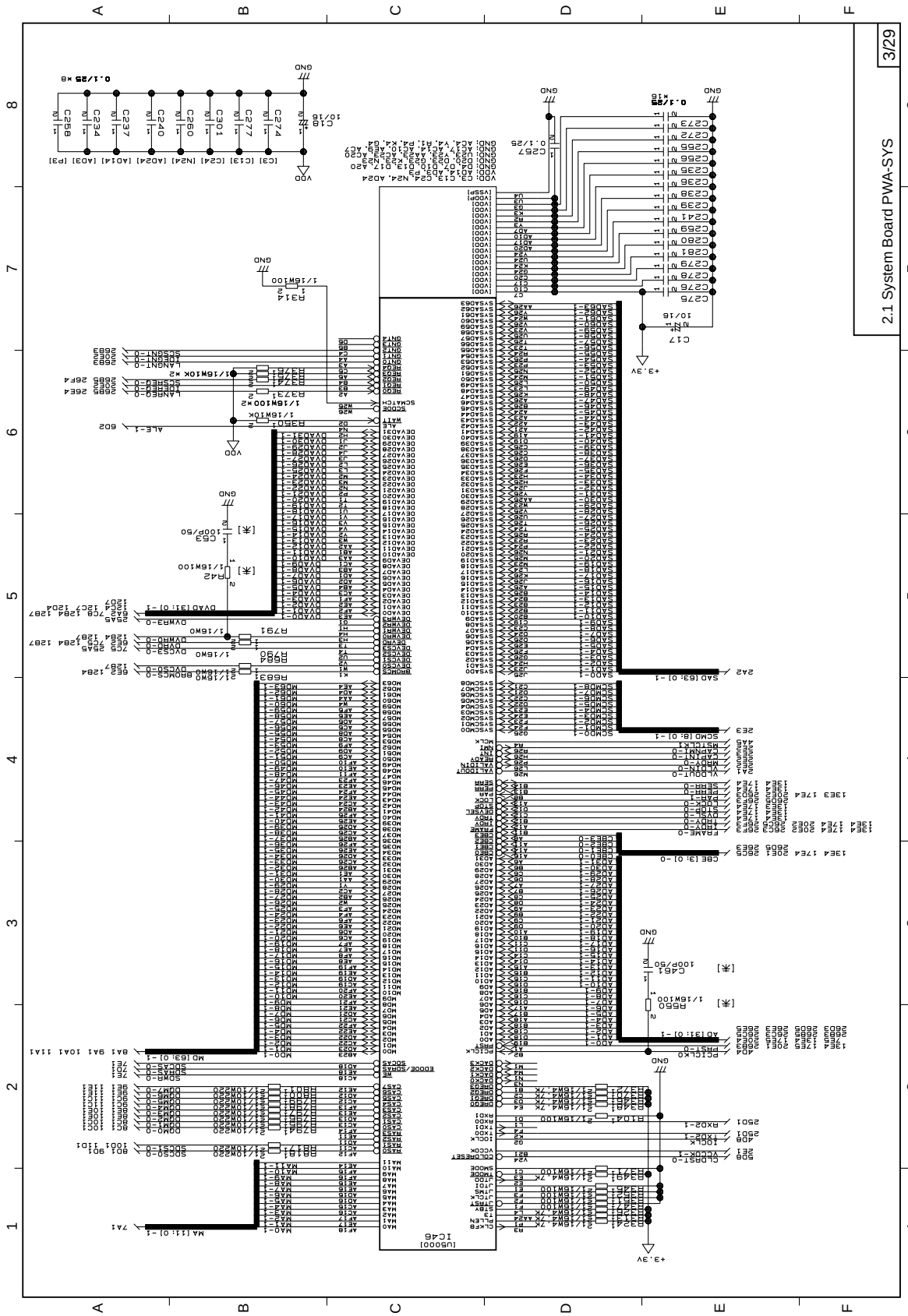
2. LOGIC CIRCUIT

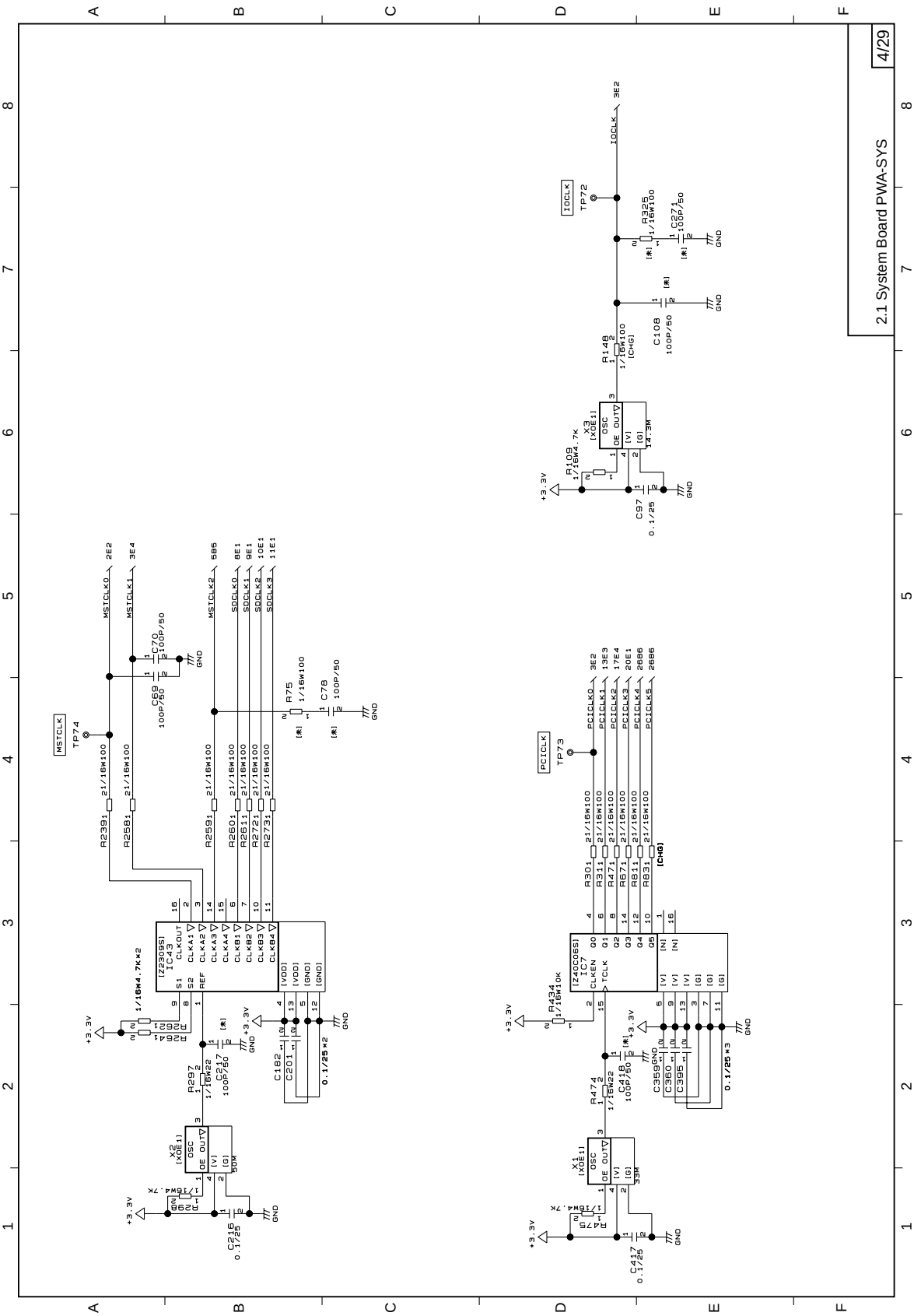
(Note : [未] [未実装] : NO MOUNT)

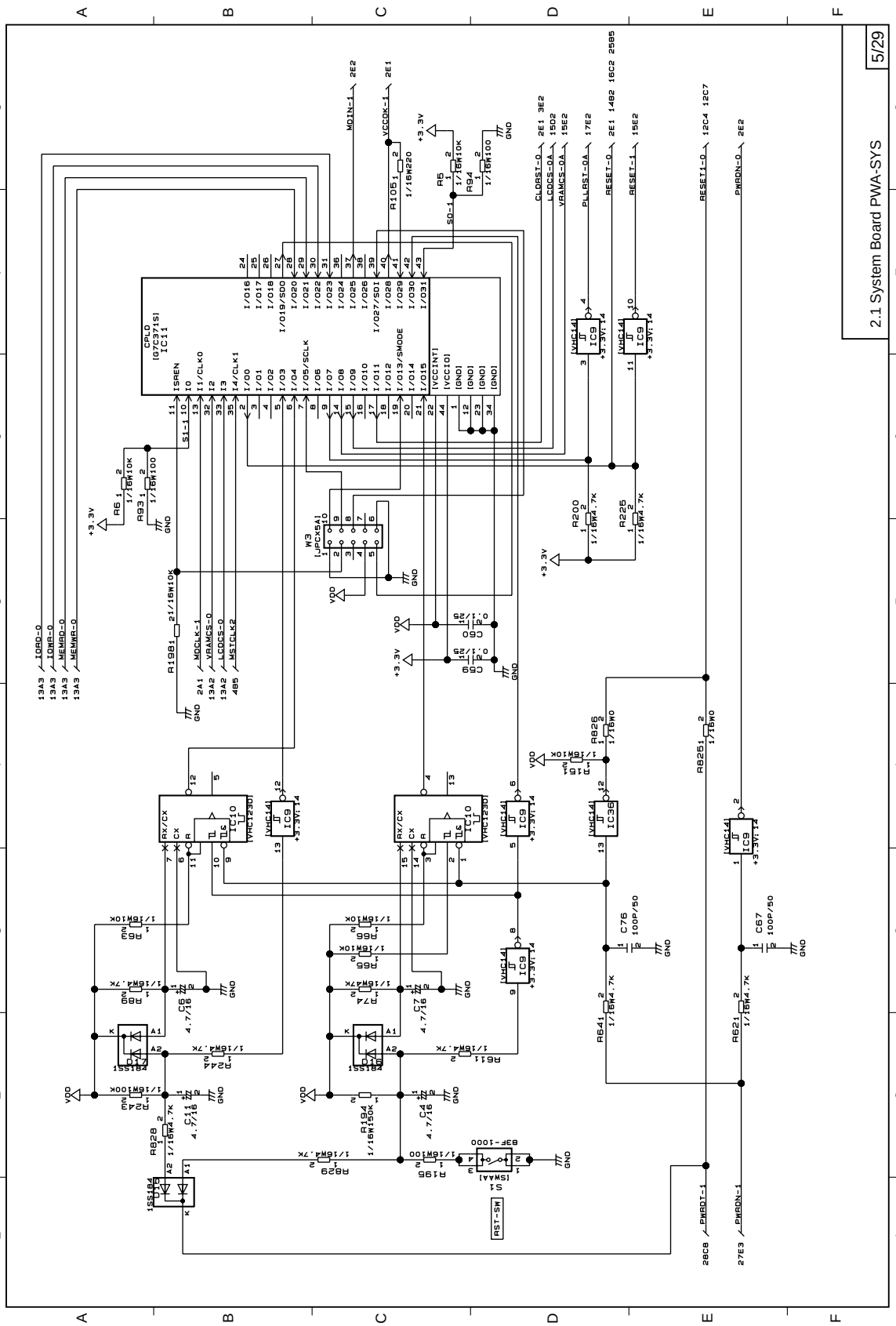
2.1 System Board (PWA-SYS) 1/29~29/29

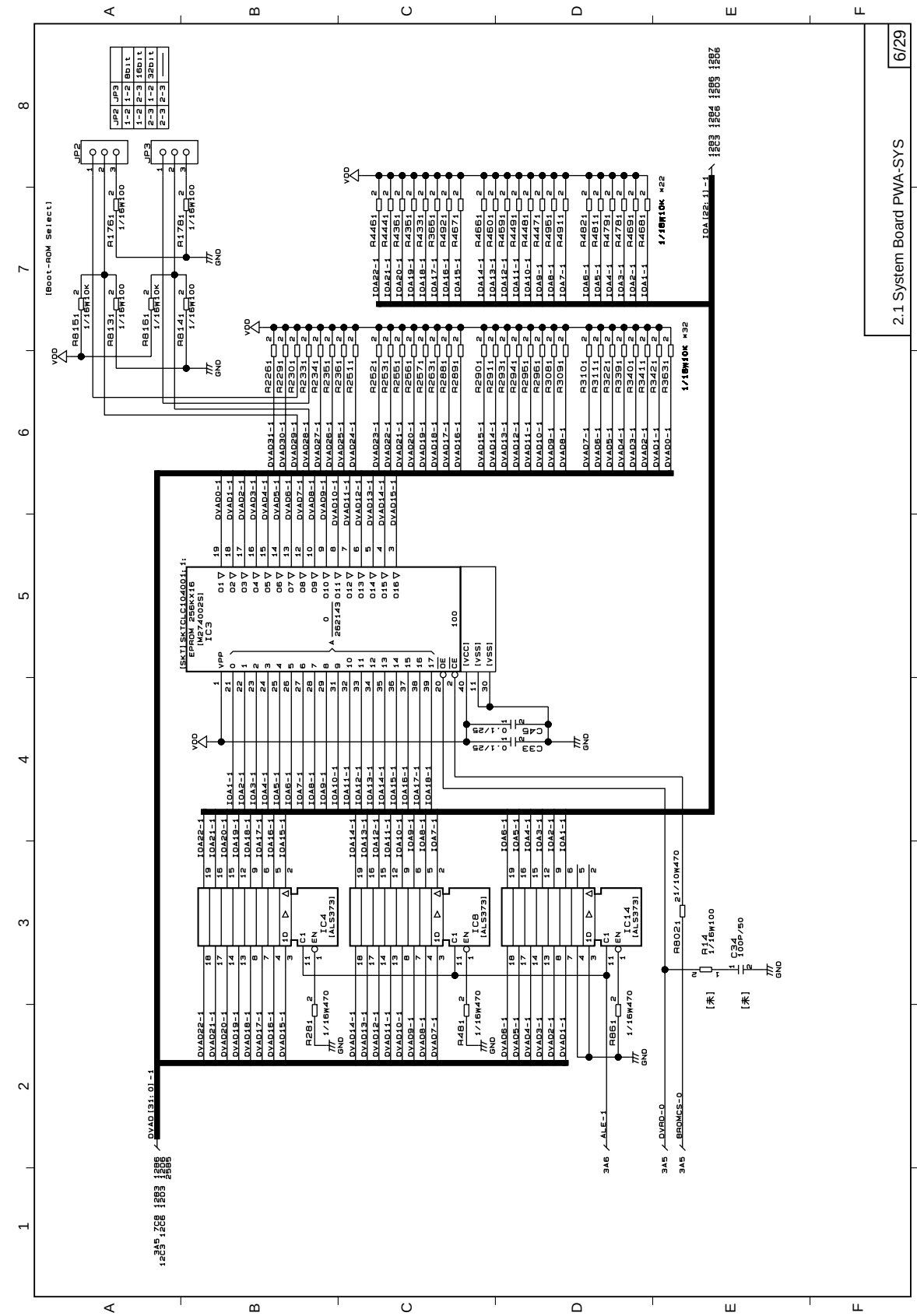


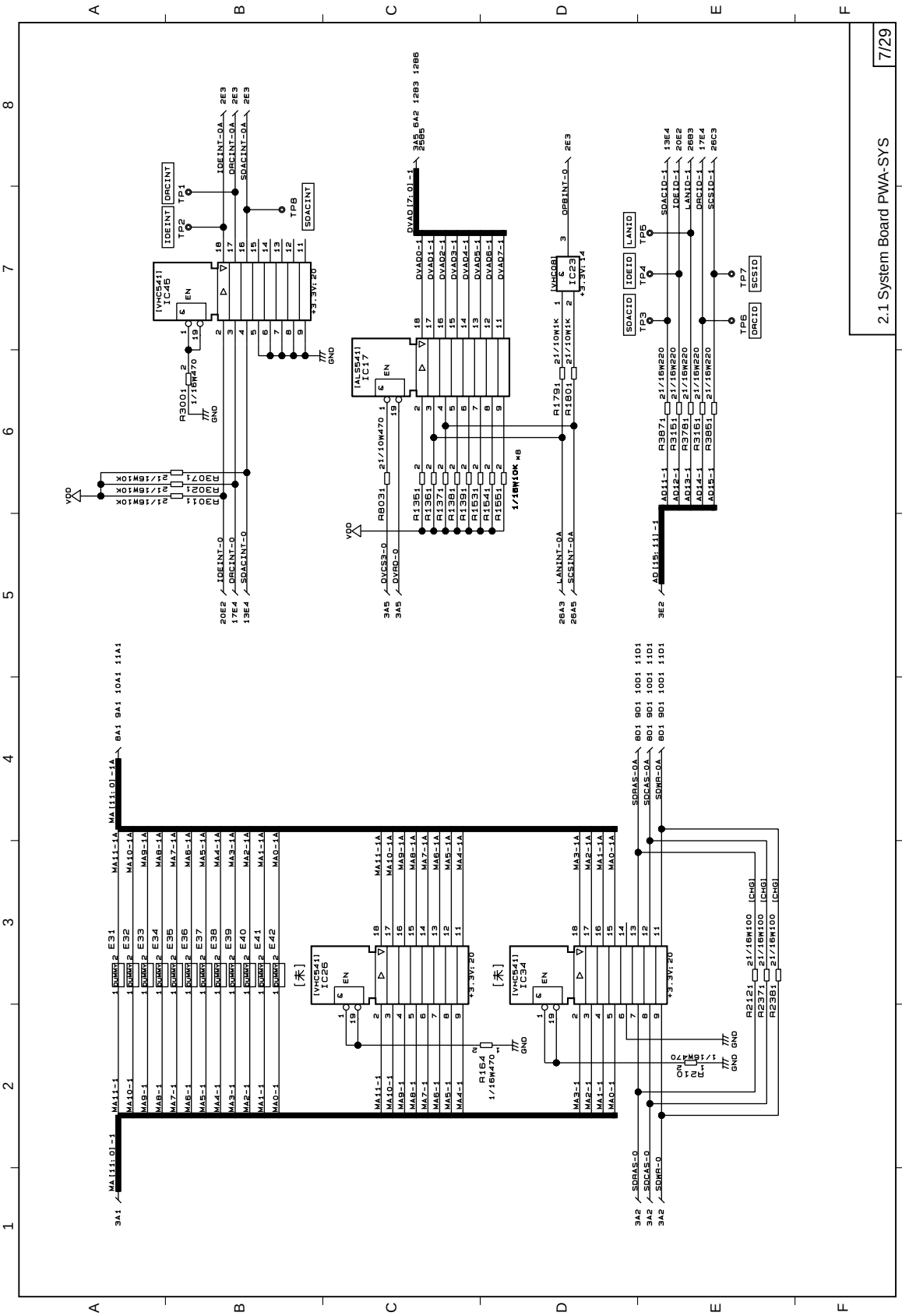

2/29
2.1 System Board PWA-SYS

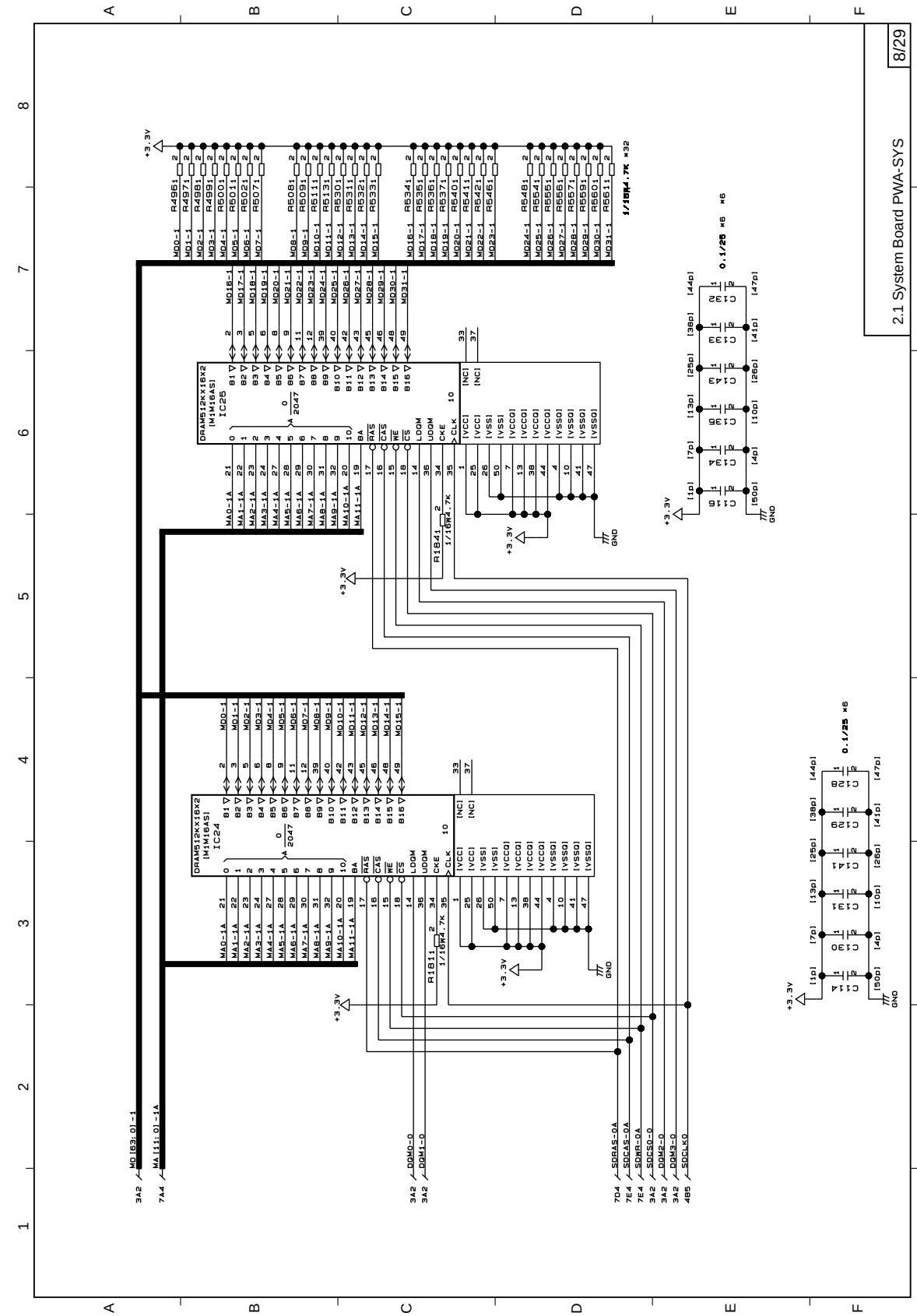

3/29
2.1 System Board PWA-SYS

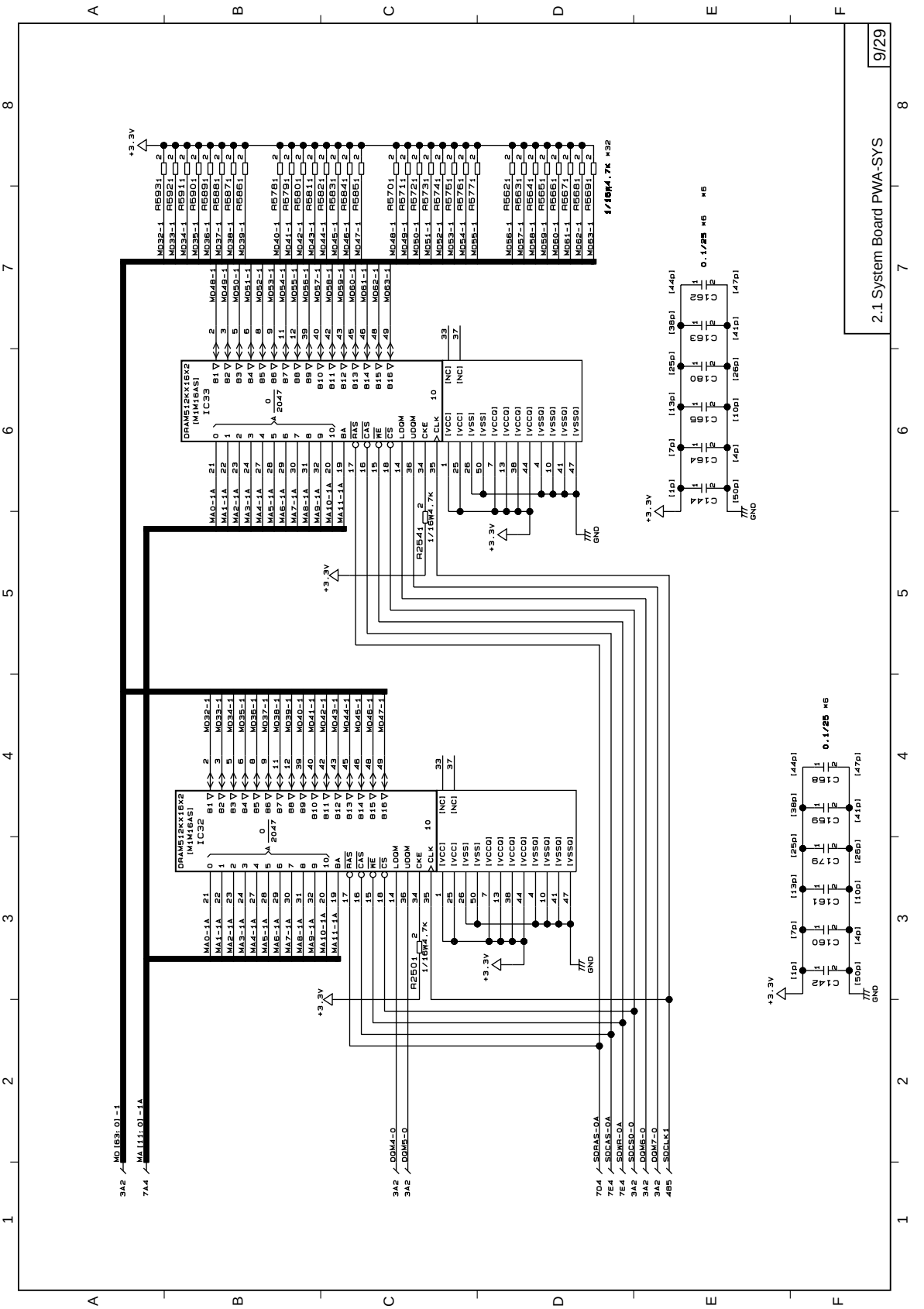

2.1 System Board PWA-SYS
4/29

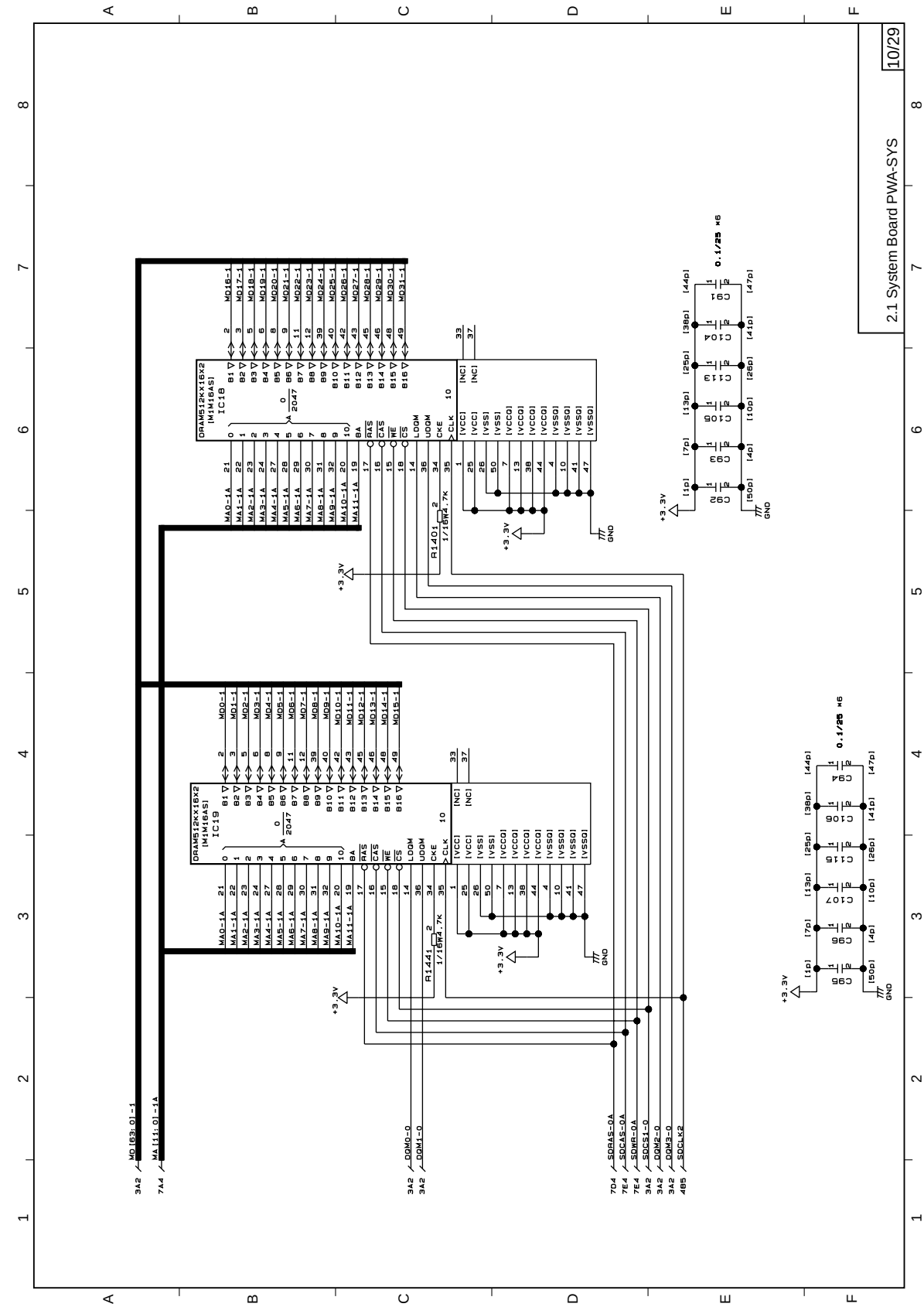

2.1 System Board PWA-SYS
5/29

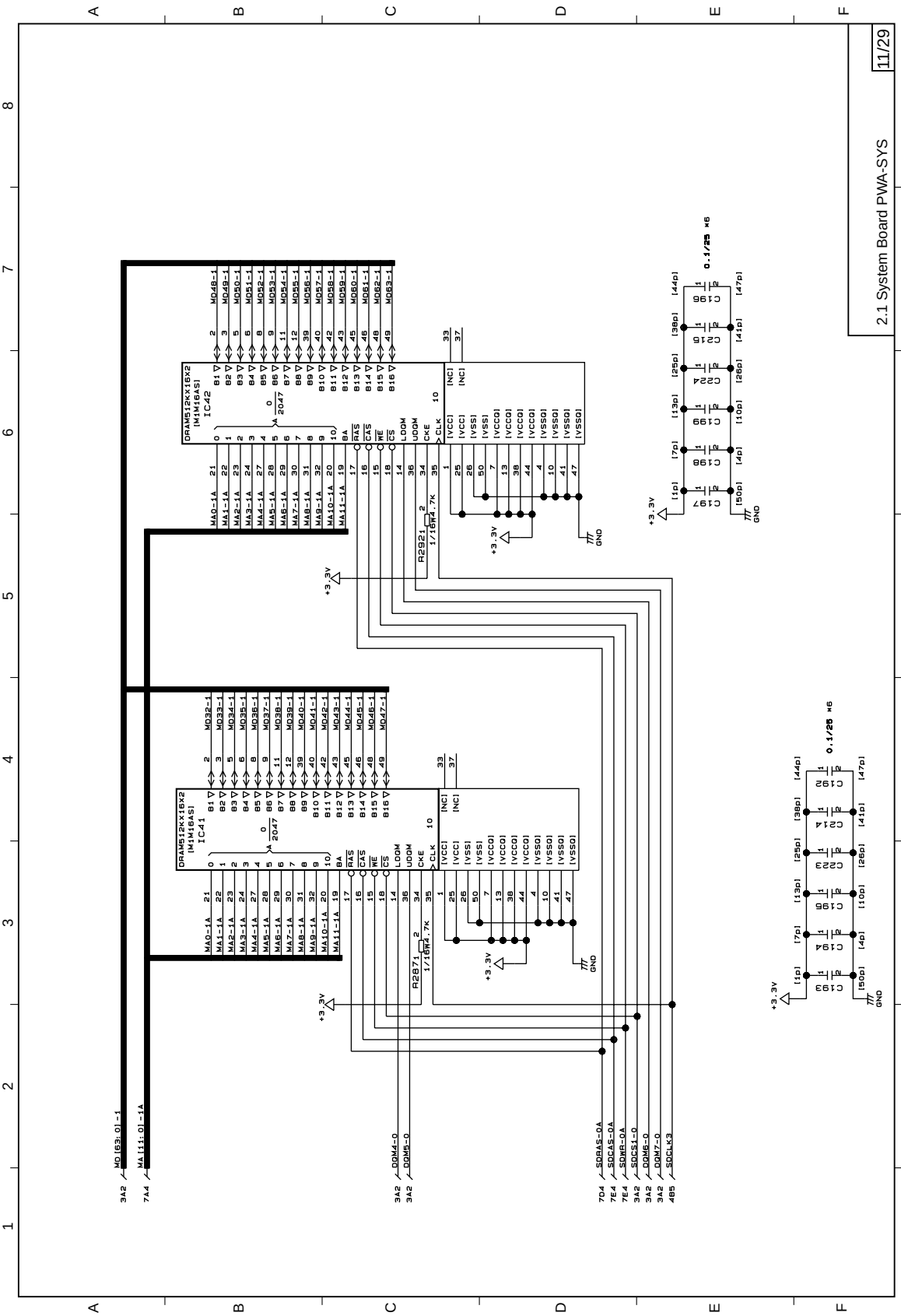

2.1 System Board PWA-SYS
6/29
[Boot-ROM Select]
JP2
JP3
1-2 1-2 8bit
1-2 2-3 16bit
2-3 1-2 32bit
2-3 2-3
VDD
GND
R1761 1/16W100
R1781 1/16W100
RB161 1/16W10K
RB131 1/16W100
RB141 1/16W100
RB151 1/16W10K
IOA[22:1]-1
1/16W10K *22
1/16W10K *32
R2261 R2291 R2301 R2331 R2341 R2351 R2361 R2511
R2621 R2531 R2551 R2561 R2571 R2581 R2591 R2671
R2901 R2911 R2931 R2941 R2961 R3081 R3091 R3101
R3111 R3221 R3391 R3401 R3411 R3421 R3631
R4461 R4441 R4361 R4351 R4331 R4651 R4671
R4661 R4601 R4591 R4491 R4481 R4471 R4951 R4911
R4821 R4811 R4791 R4781 R4691 R4681
DVAD31-1 DVAD30-1 DVAD29-1 DVAD28-1 DVAD27-1 DVAD26-1 DVAD25-1 DVAD24-1
DVAD23-1 DVAD22-1 DVAD21-1 DVAD20-1 DVAD19-1 DVAD18-1 DVAD17-1 DVAD16-1
DVAD15-1 DVAD14-1 DVAD13-1 DVAD12-1 DVAD11-1 DVAD10-1 DVAD9-1 DVAD8-1
DVAD7-1 DVAD6-1 DVAD5-1 DVAD4-1 DVAD3-1 DVAD2-1 DVAD1-1 DVAD0-1
DVAD[31:0]-1
[SKHISKTGC14(40)]:
EPROM 256Kx16
[M27400251
IC13
VPP
A 262143
[VCC]
[VSS]
[VSS]
C33 0.1/25
C4 4P
C2 4P
IOA1-1 IOA2-1 IOA3-1 IOA4-1 IOA5-1 IOA6-1 IOA7-1 IOA8-1 IOA9-1 IOA10-1 IOA11-1 IOA12-1 IOA13-1 IOA14-1 IOA15-1 IOA16-1 IOA17-1 IOA18-1
IOA22-1 IOA21-1 IOA20-1 IOA19-1 IOA18-1 IOA17-1 IOA16-1 IOA15-1
IOA14-1 IOA13-1 IOA12-1 IOA11-1 IOA10-1 IOA9-1 IOA8-1 IOA7-1
IOA6-1 IOA5-1 IOA4-1 IOA3-1 IOA2-1 IOA1-1
IC4 [ALS373]
IC8 [ALS373]
IC14 [ALS373]
R281 1/16W470
R481 1/16W470
R861 1/16W470
RB021 21/10W470
R14 1/16W100
C34 100P/50
[未]
[未]
3A5 7C8 1203 1206
3A5 1206 1203 1206 1205
3A6 ALE-1
3A5 DVBD-0
3A5 BROMCS-0
1203 1206 1204 1206 1203 1206 1207

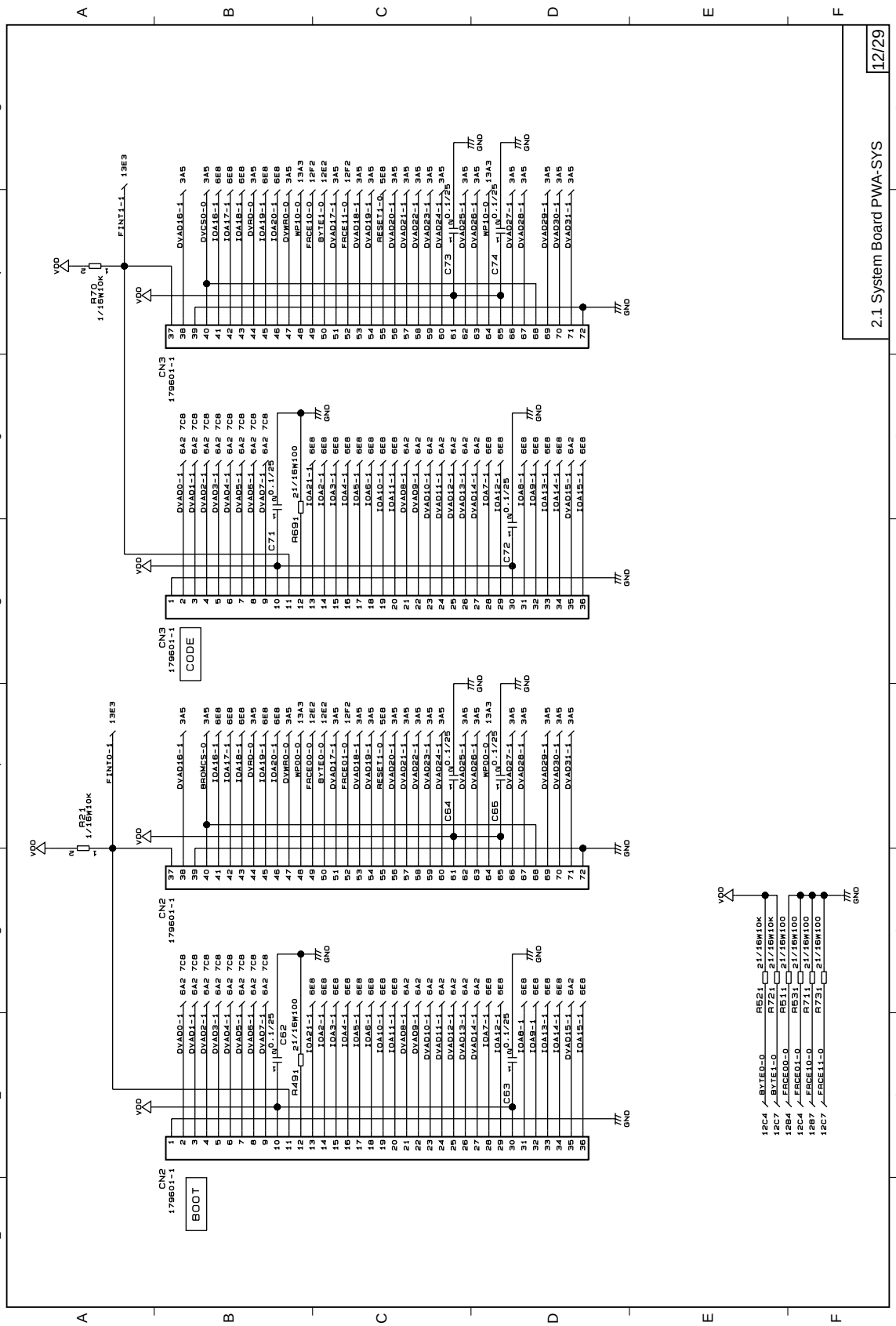

2.1 System Board PWA-SYS
7/29

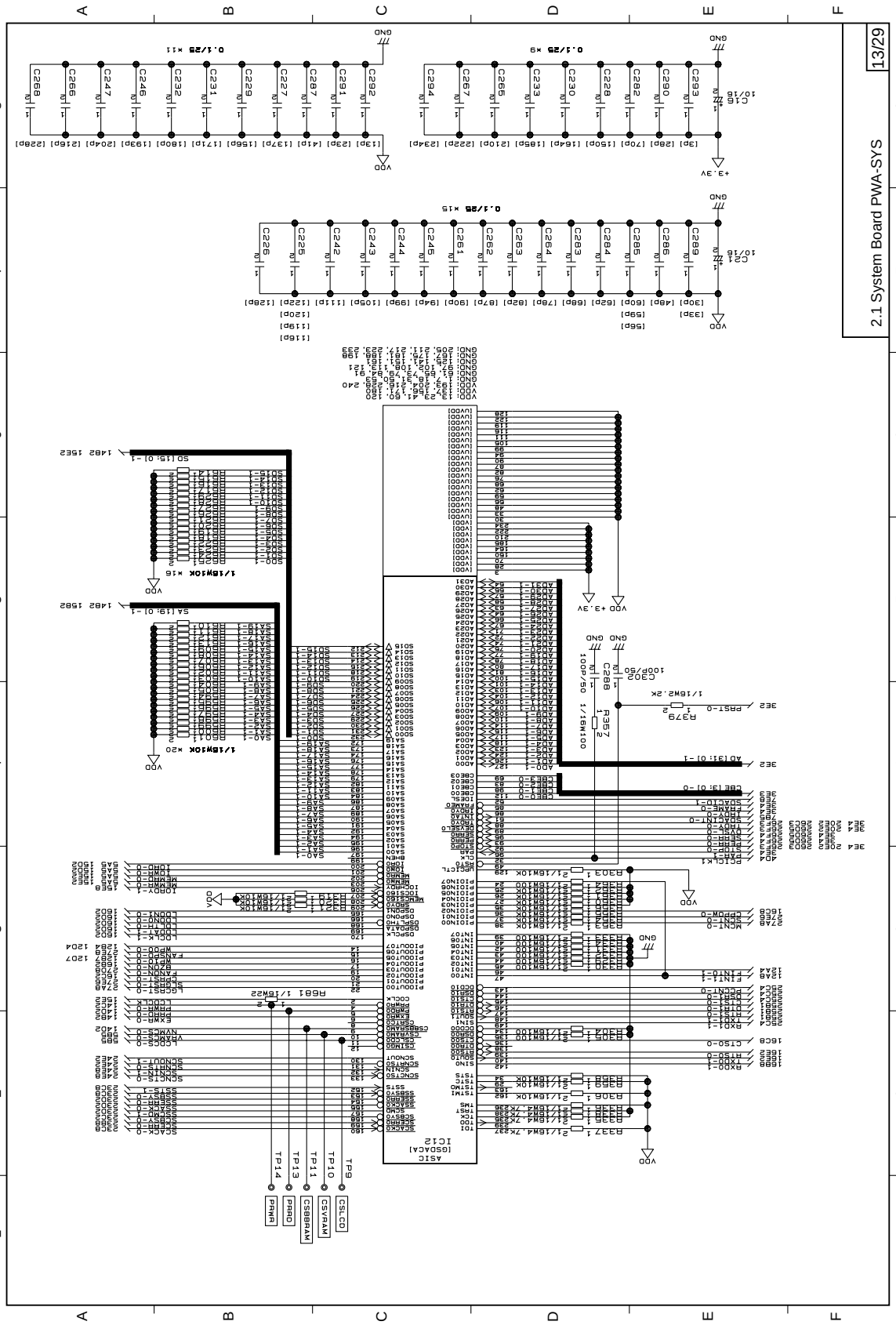

2.1 System Board PWA-SYS
8/29
DRAM512Kx16x2
[M1M16A5]
IC24
IC25
R1841
1/16W4.7K
0.1/25 ×6
+3.3V
GND
MD63-0 1-1
MA11-0 1-1A
DQM0-0
DQM1-0
SDRAS-0A
SDCAS-0A
SDWE-0A
SDCS0-0
DQM2-0
DQM3-0
SDCLK0

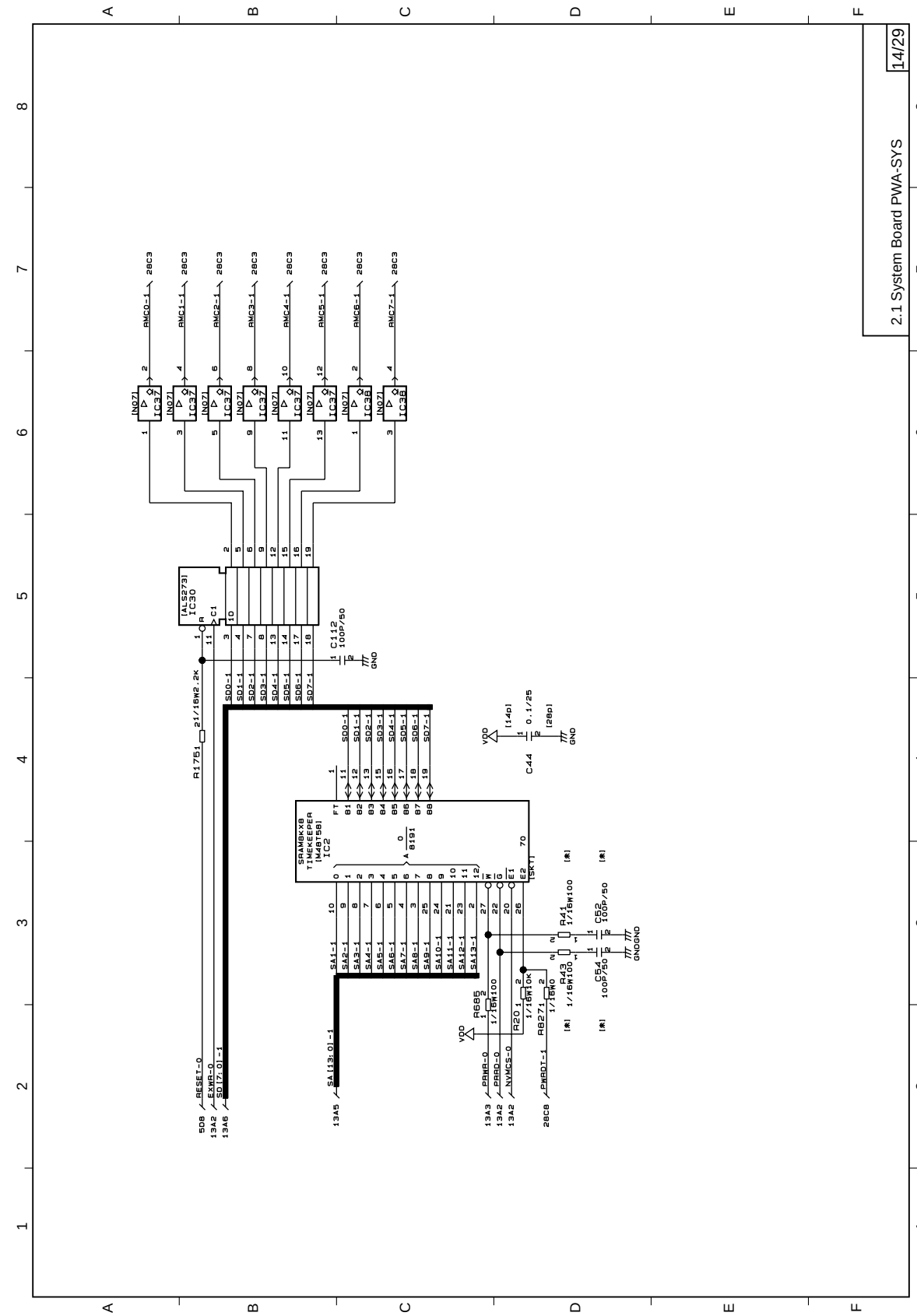

2.1 System Board PWA-SYS
9/29
DRAM512Kx16x2
[M1M16A5]
IC32
IC33
+3.3V
GND
R2541
R2501
1/16W4.7K
1/16W4.7K x32
0.1/25 x6
MD[63:0]-1
MA[11:0]-1A
DQM4-0
DQM5-0
DQM6-0
DQM7-0
SDRAS-0A
SDCAS-0A
SDWE-0A
SDCS0-0
SDCLK1

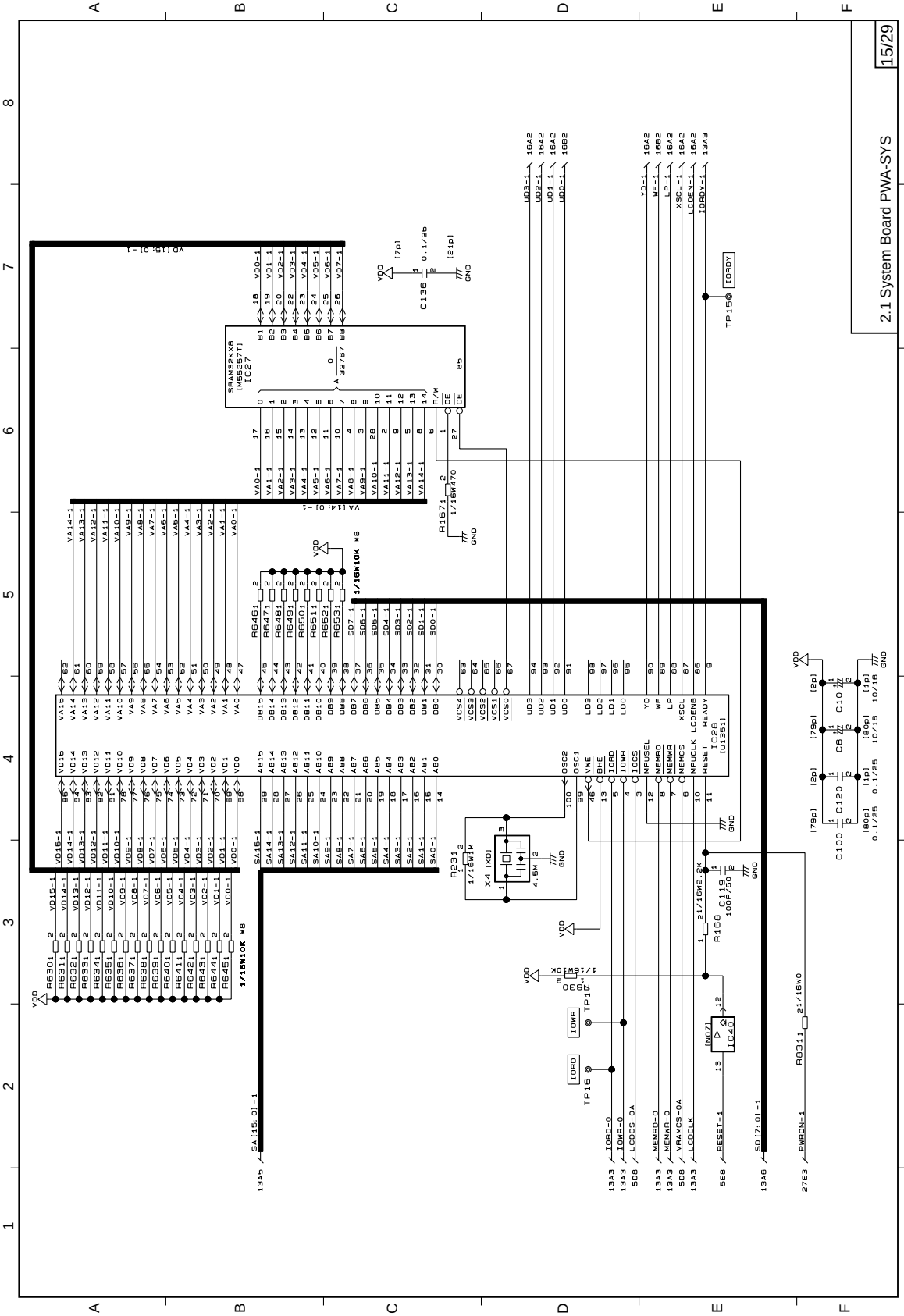

2.1 System Board PWA-SYS
10/29
DRAM512Kx16x2
(M1M16AS)
IC18
IC19
R1401
1/16W
4.7K
0.1/25 ×6
+3.3V
GND
MD15-1
MD14-1
MD13-1
MD12-1
MD11-1
MD10-1
MD9-1
MD8-1
MD7-1
MD6-1
MD5-1
MD4-1
MD3-1
MD2-1
MD1-1
MD0-1
MD31-1
MD30-1
MD29-1
MD28-1
MD27-1
MD26-1
MD25-1
MD24-1
MD23-1
MD22-1
MD21-1
MD20-1
MD19-1
MD18-1
MD17-1
MD16-1
MD[63:0]-1
MA[11:0]-1A
DQM0-0
DQM1-0
SDRAS-0A
SDCAS-0A
SDWR-0A
SDCS1-0
DQM2-0
DQM3-0
SDCLK2

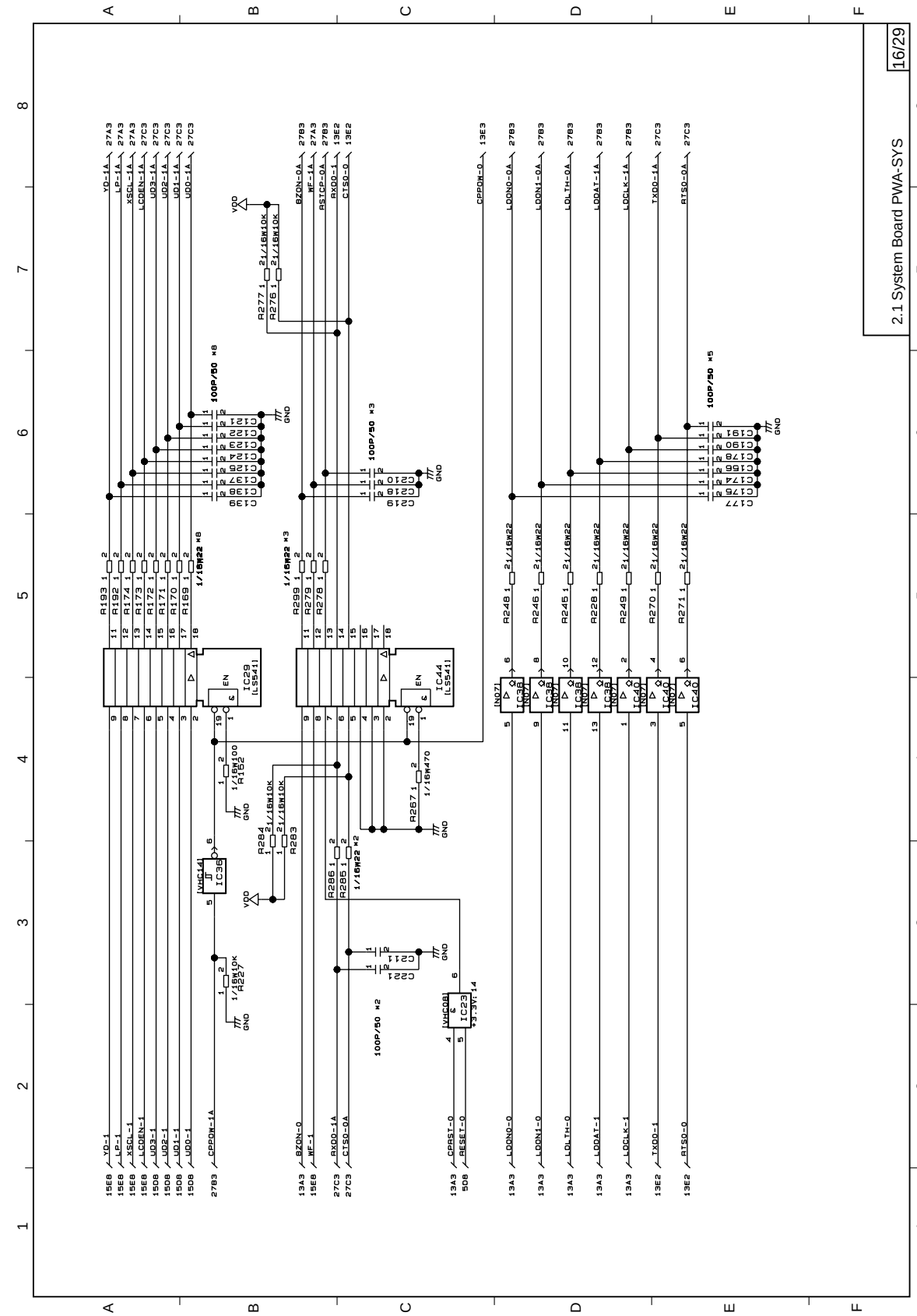

2.1 System Board PWA-SYS
11/29
DRAM512Kx16X2
(M1M16AS)
IC41
IC42
MD63-01-1
MA11-01-1A
R2871
R2921
1/16W4.7K
0.1/25 x6
+3.3V
GND
DQM4-0
DQM5-0
DQM6-0
DQM7-0
SDRAS-0A
SDCAS-0A
SDWE-0A
SDCS1-0
SDCLK3

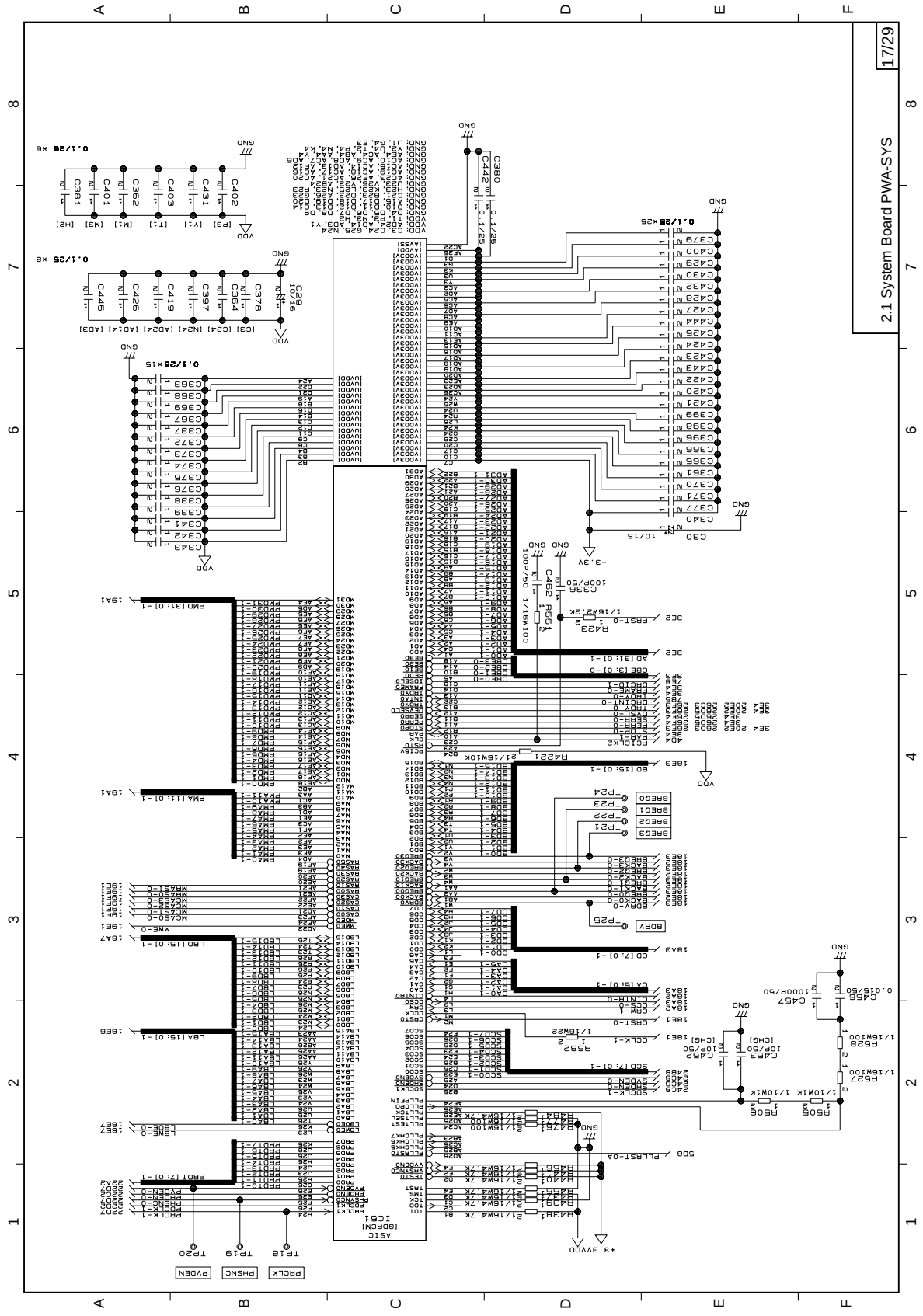

2.1 System Board PWA-SYS
12/29
BOOT
CODE
CN2
179601-1
CN3
179601-1
R21
1/16W10K
R70
1/16W10K
FINT0-1
FINT1-1
13E3
VDD
GND
C62
C63
C64
C65
C71
C72
C73
C74
R491
R691
21/16W100
R521
R721
R511
R531
R711
R731
21/16W10K
21/16W100
BYTE0-0
BYTE1-0
FRCE00-0
FRCE01-0
FRCE10-0
FRCE11-0

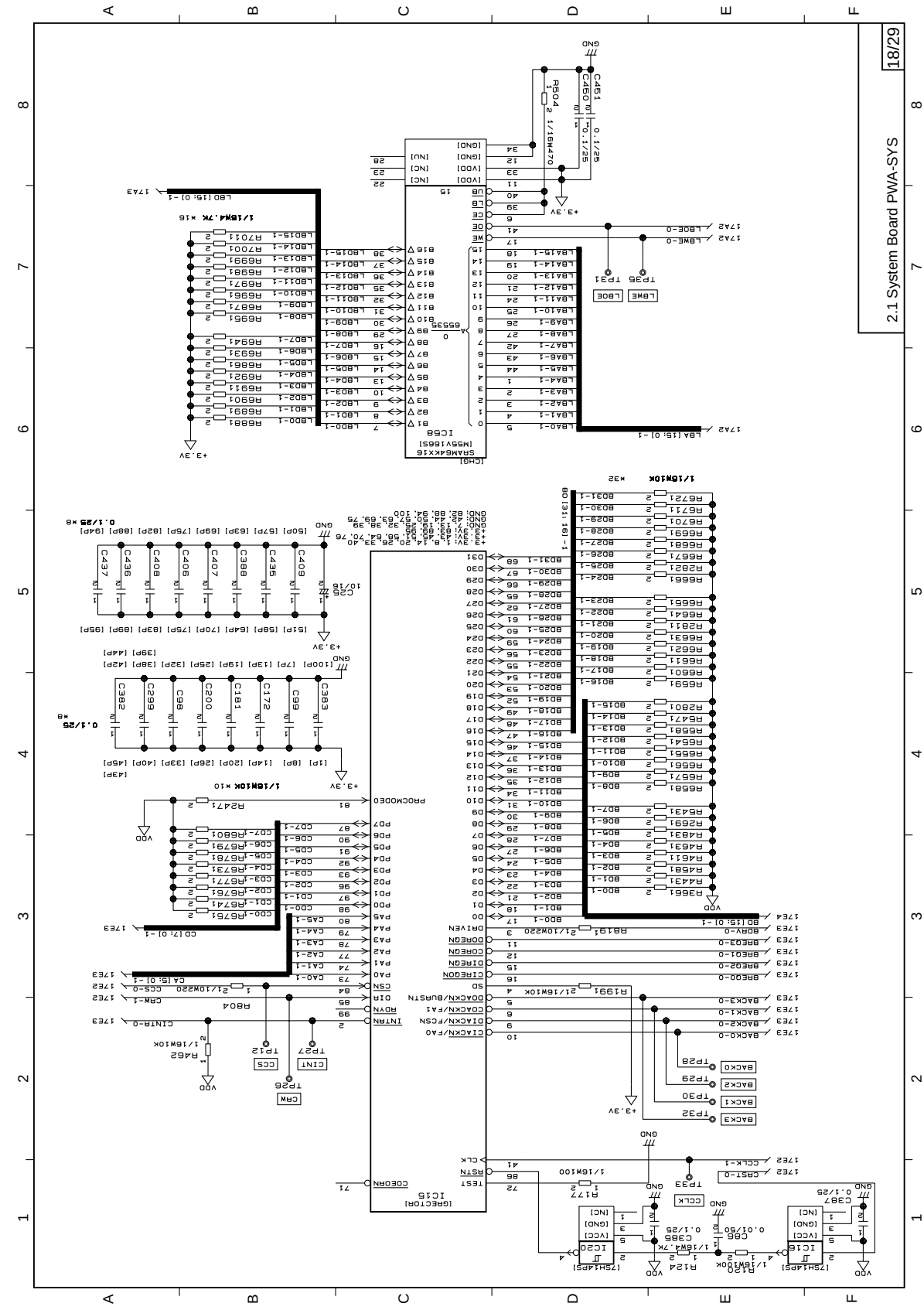

2.1 System Board PWA-SYS
13/29
ASIC
IC12
TP14
TP13
TP11
TP10
TP9
PRWR
PRRD
CSSBRAM
CSVRAM
CSLCD

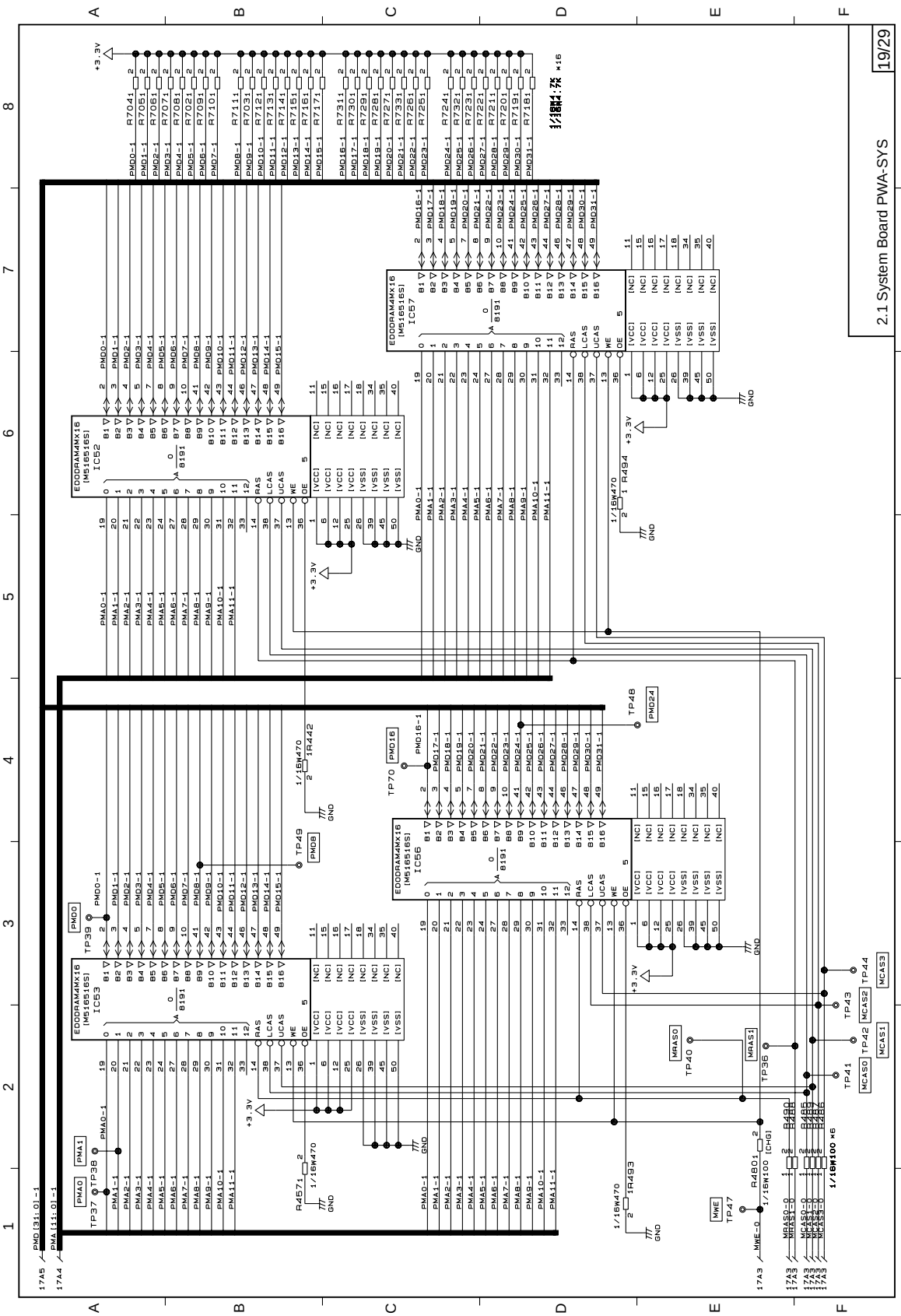

2.1 System Board PWA-SYS
14/29

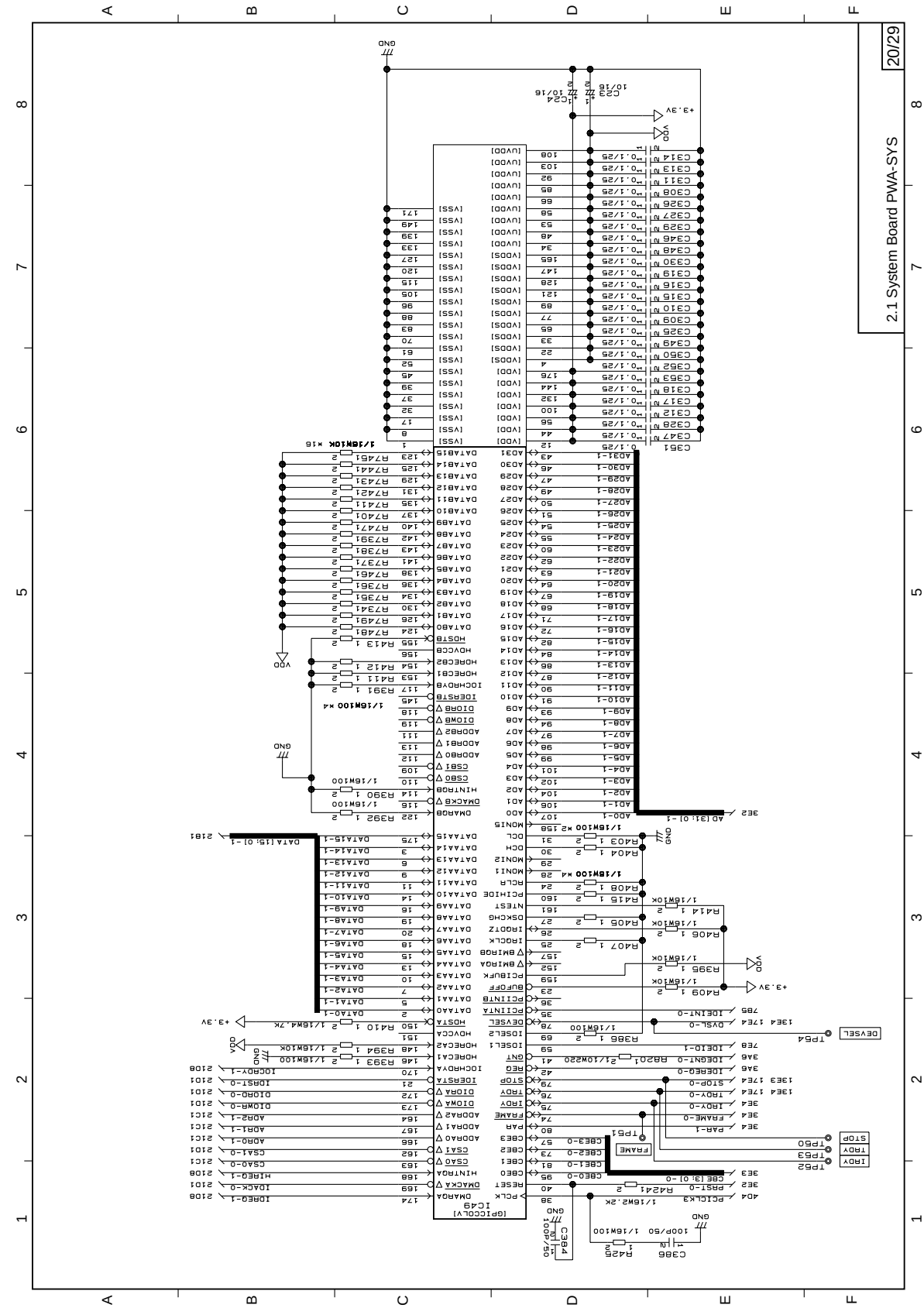

2.1 System Board PWA-SYS
15/29

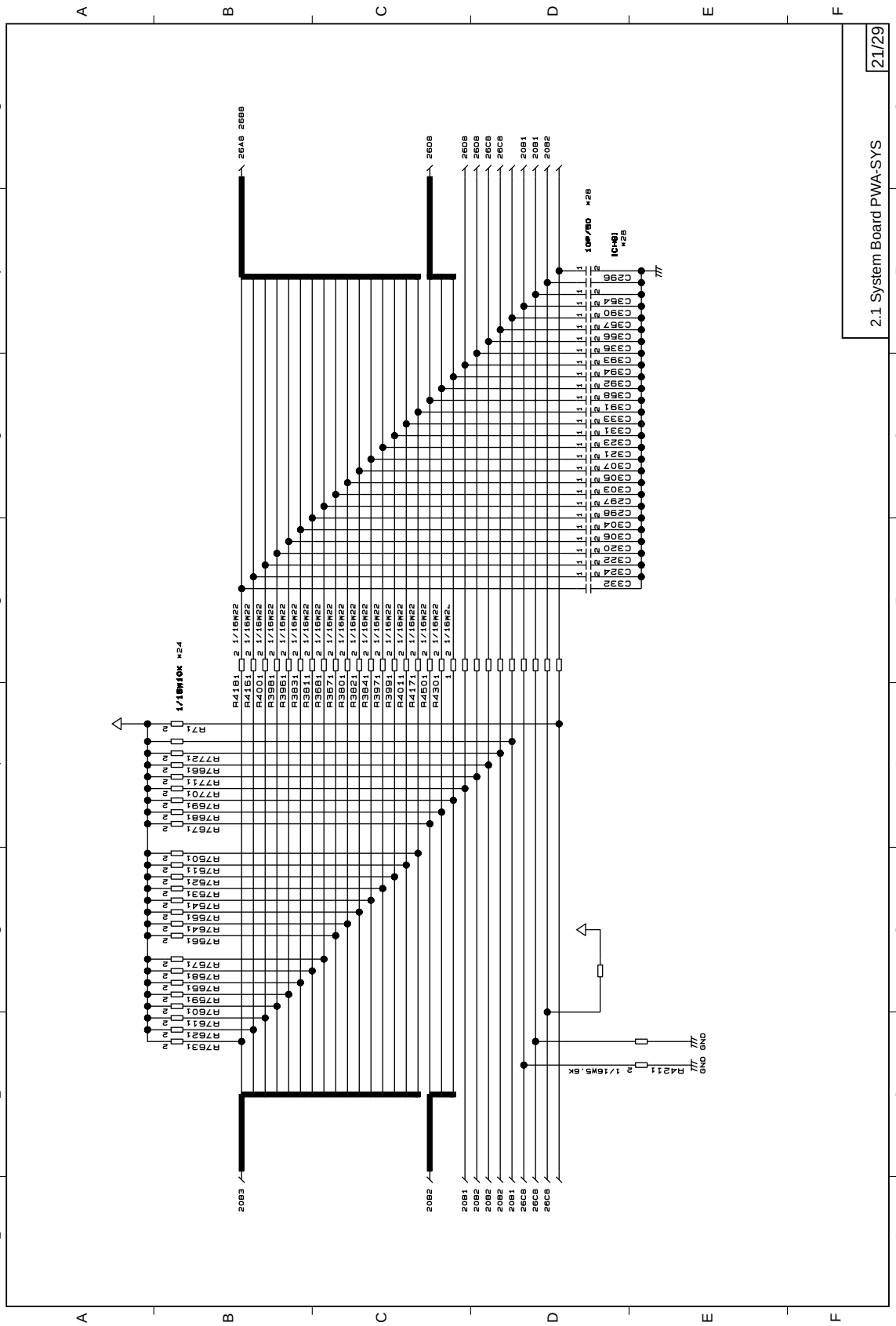

2.1 System Board PWA-SYS
16/29

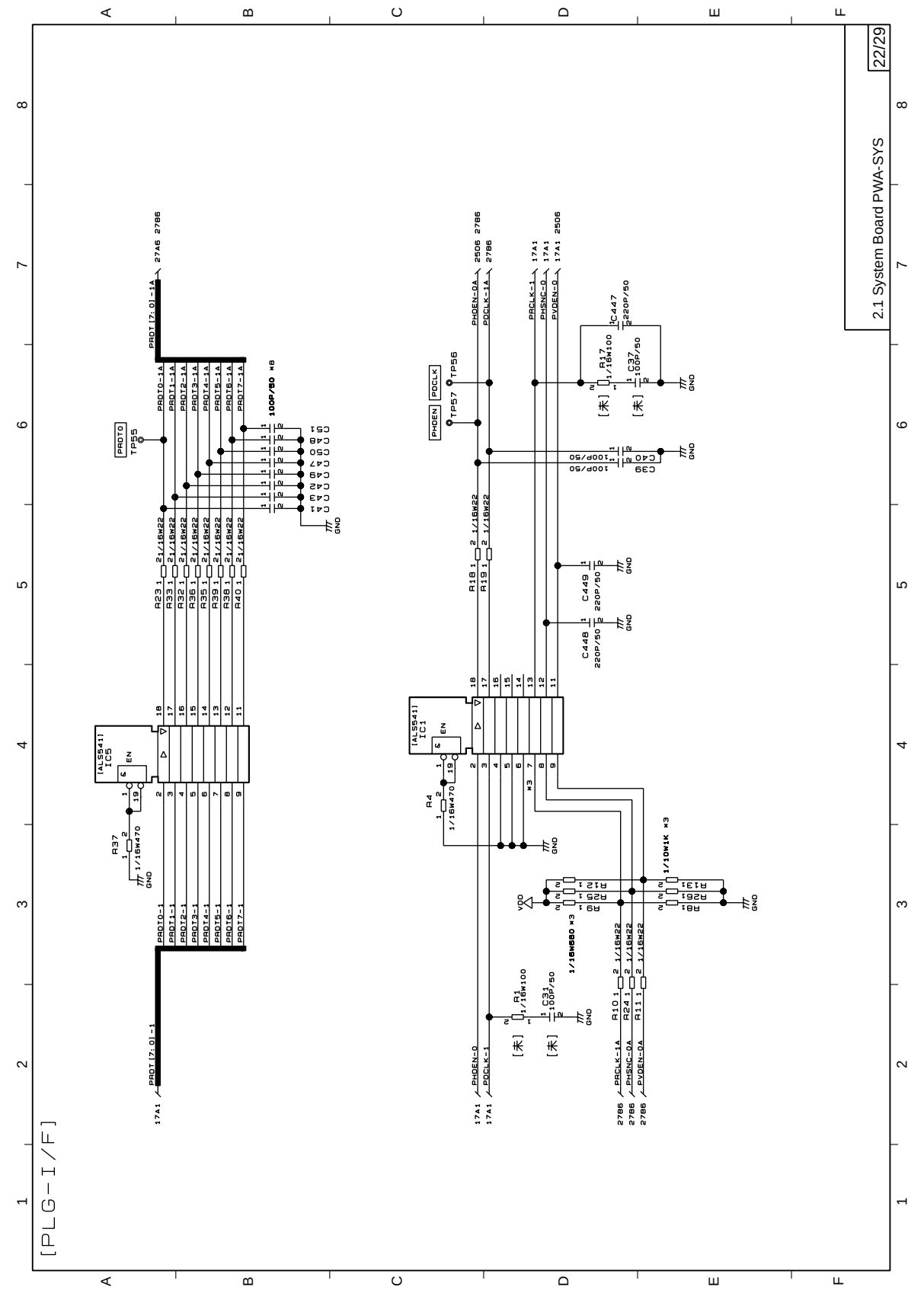

2.1 System Board PWA-SYS
17/29

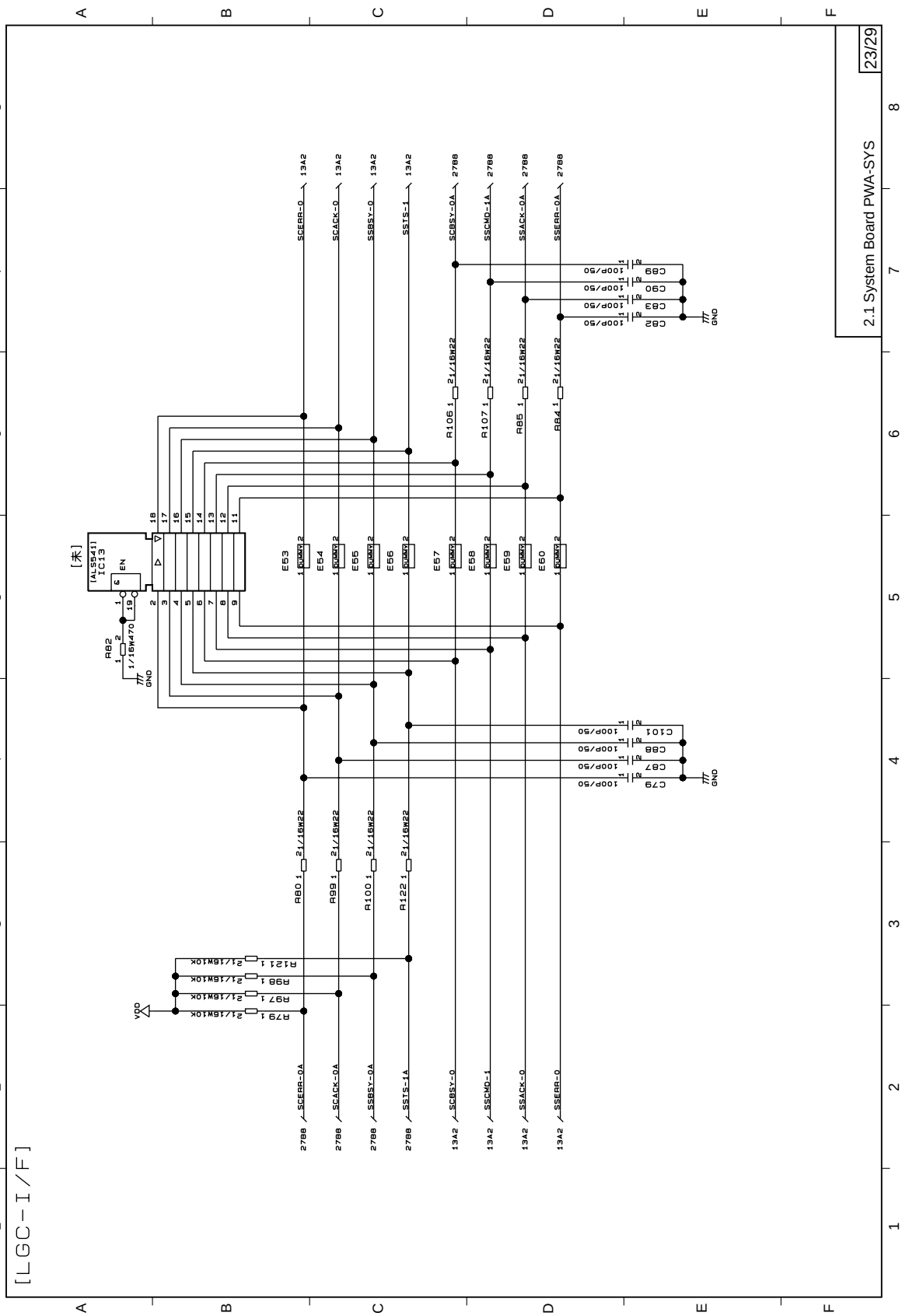

18/29
2.1 System Board PWA-SYS

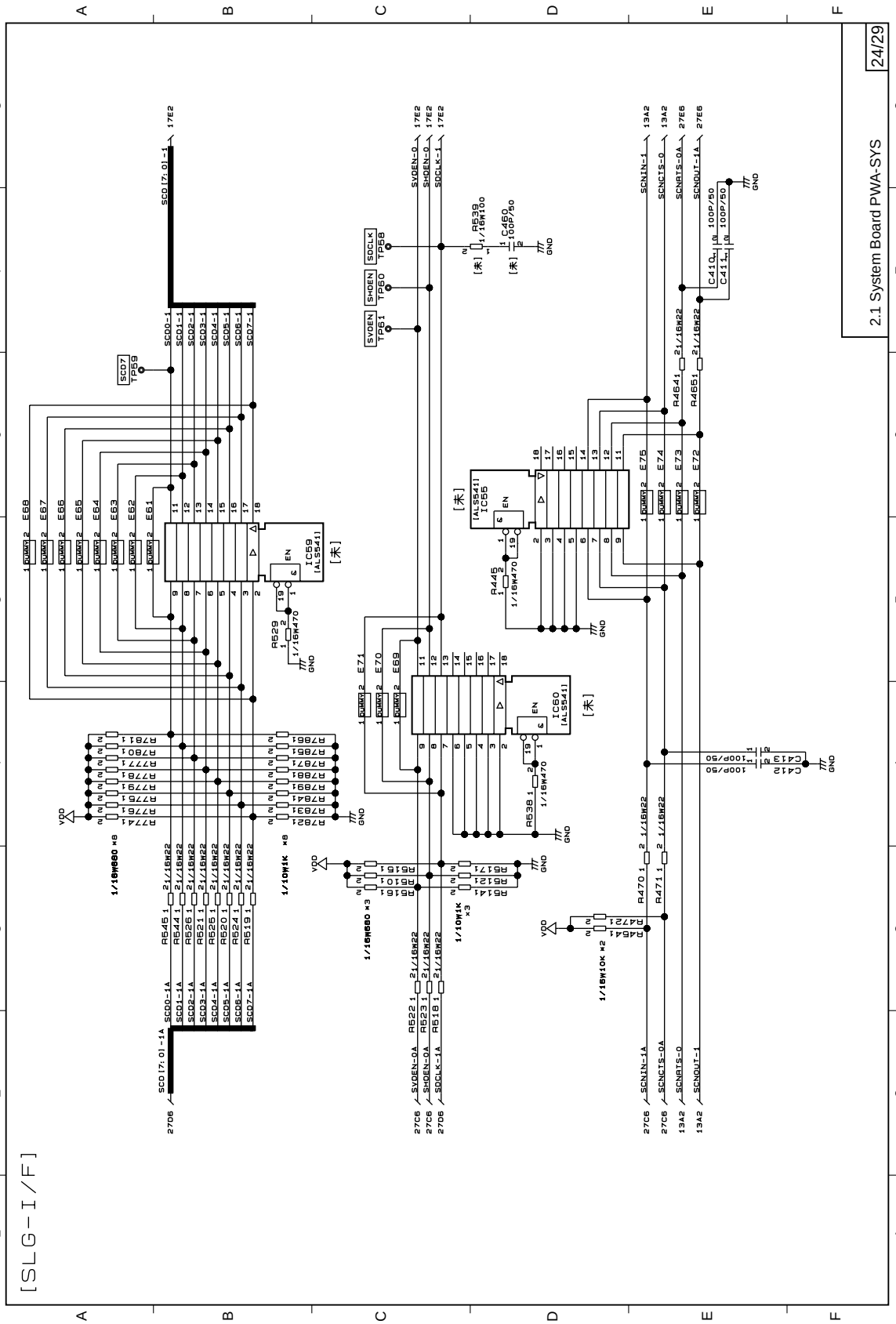

2.1 System Board PWA-SYS
19/29

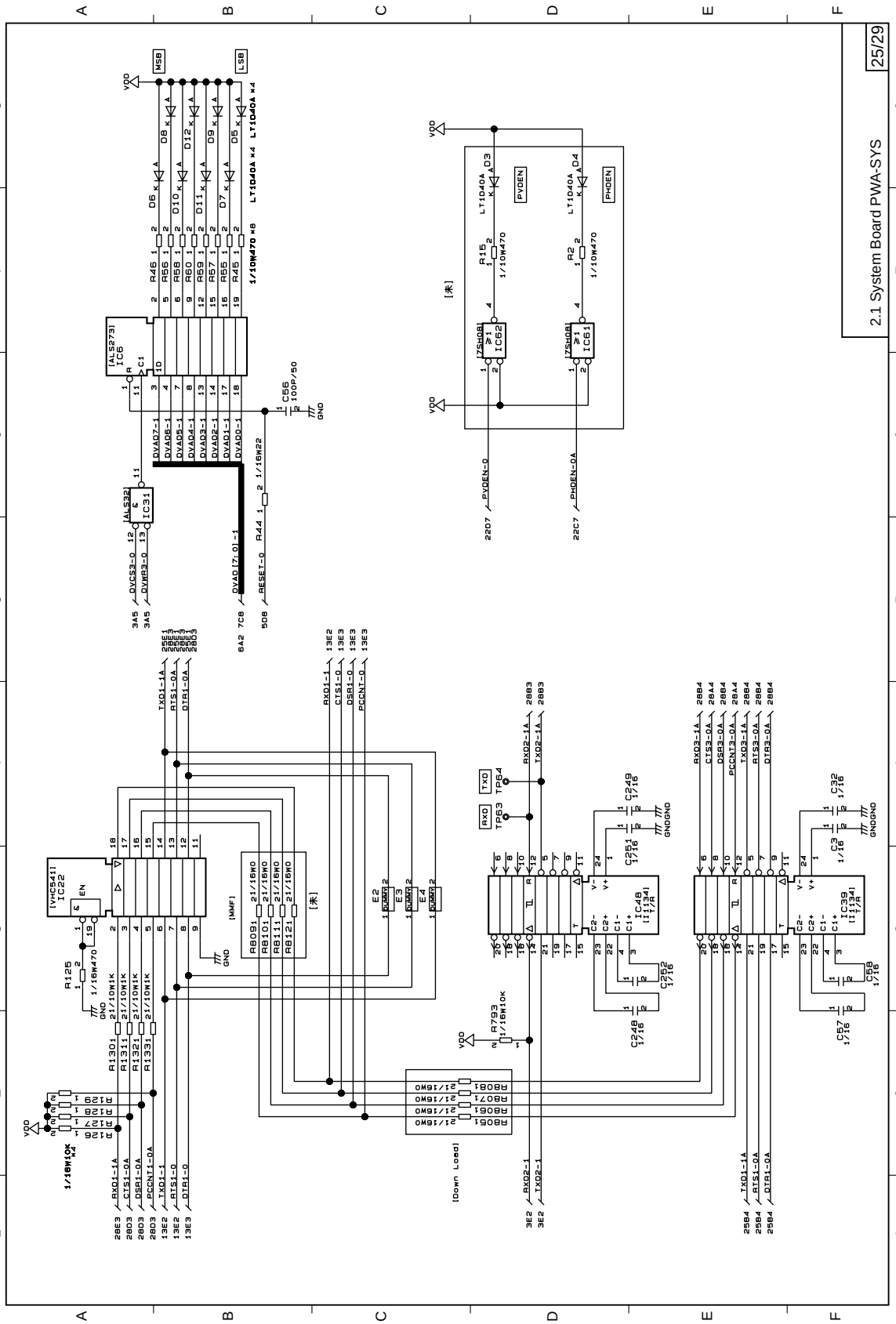

2.1 System Board PWA-SYS
20/29

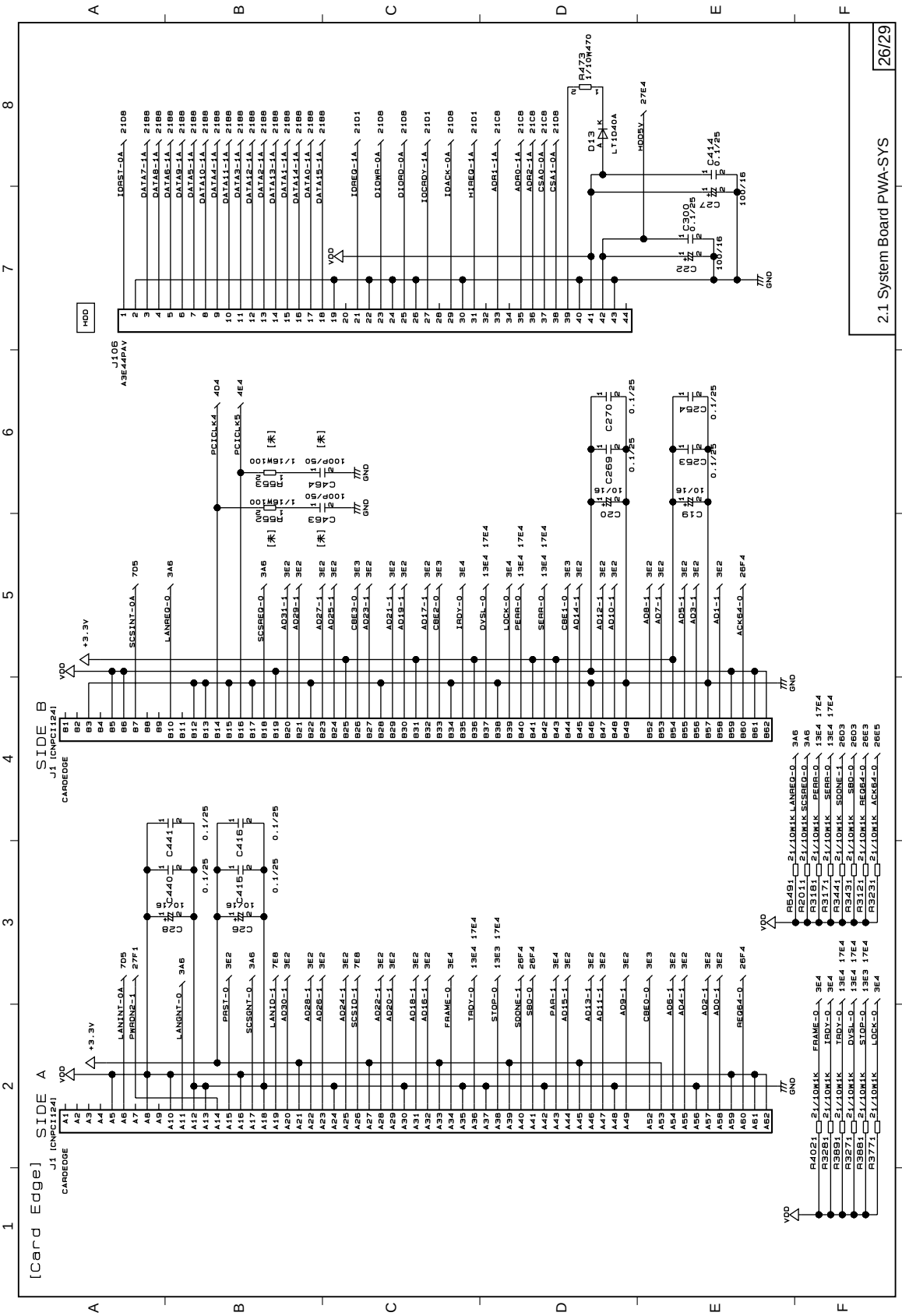

2.1 System Board PWA-SYS
21/29

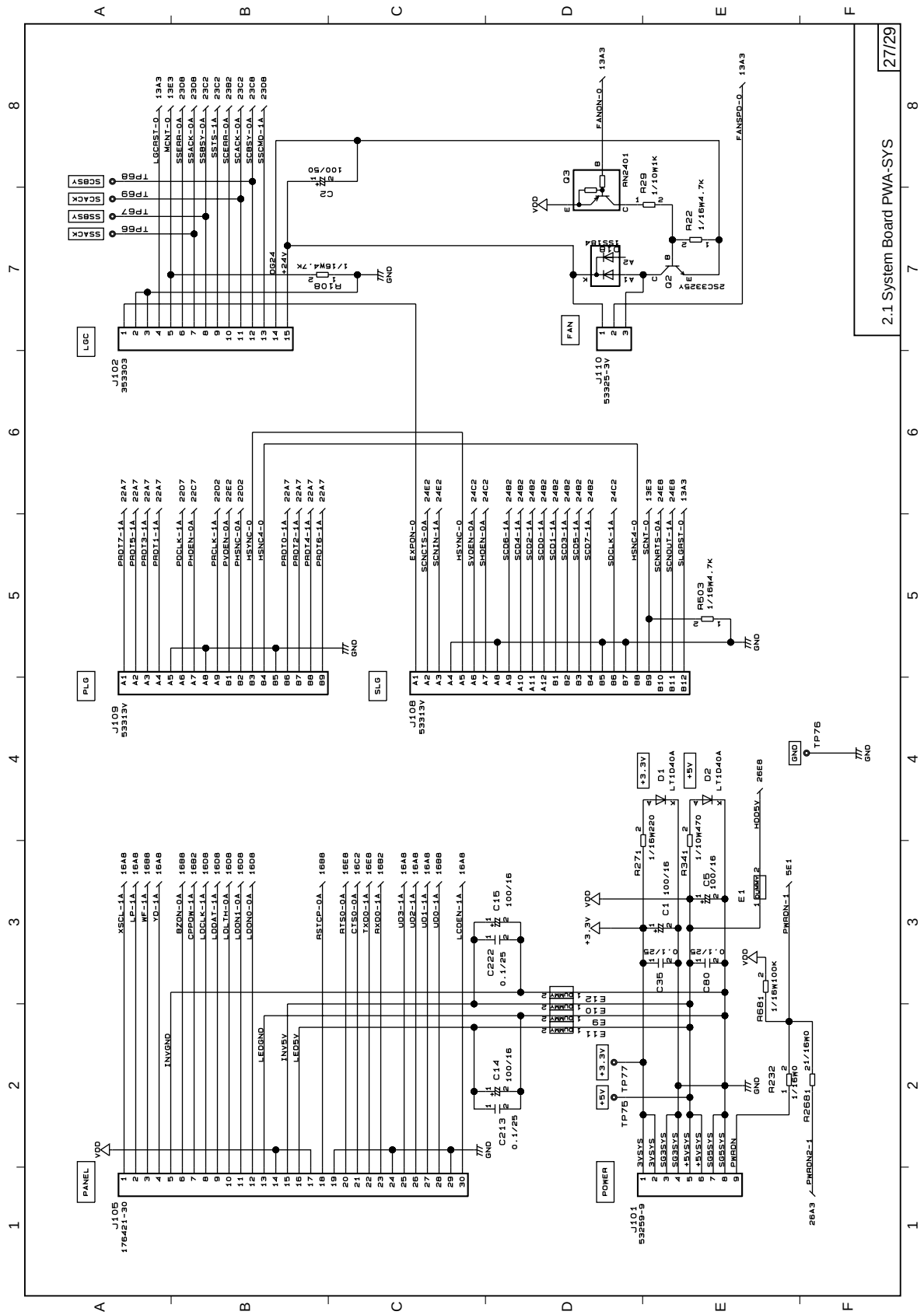

[PLG-I/F]
2.1 System Board PWA-SYS
22/29
IC5
IC1
TPS5
TPS6
TPS7
PROTO
PHDEN
PDCLK
GND
VDD

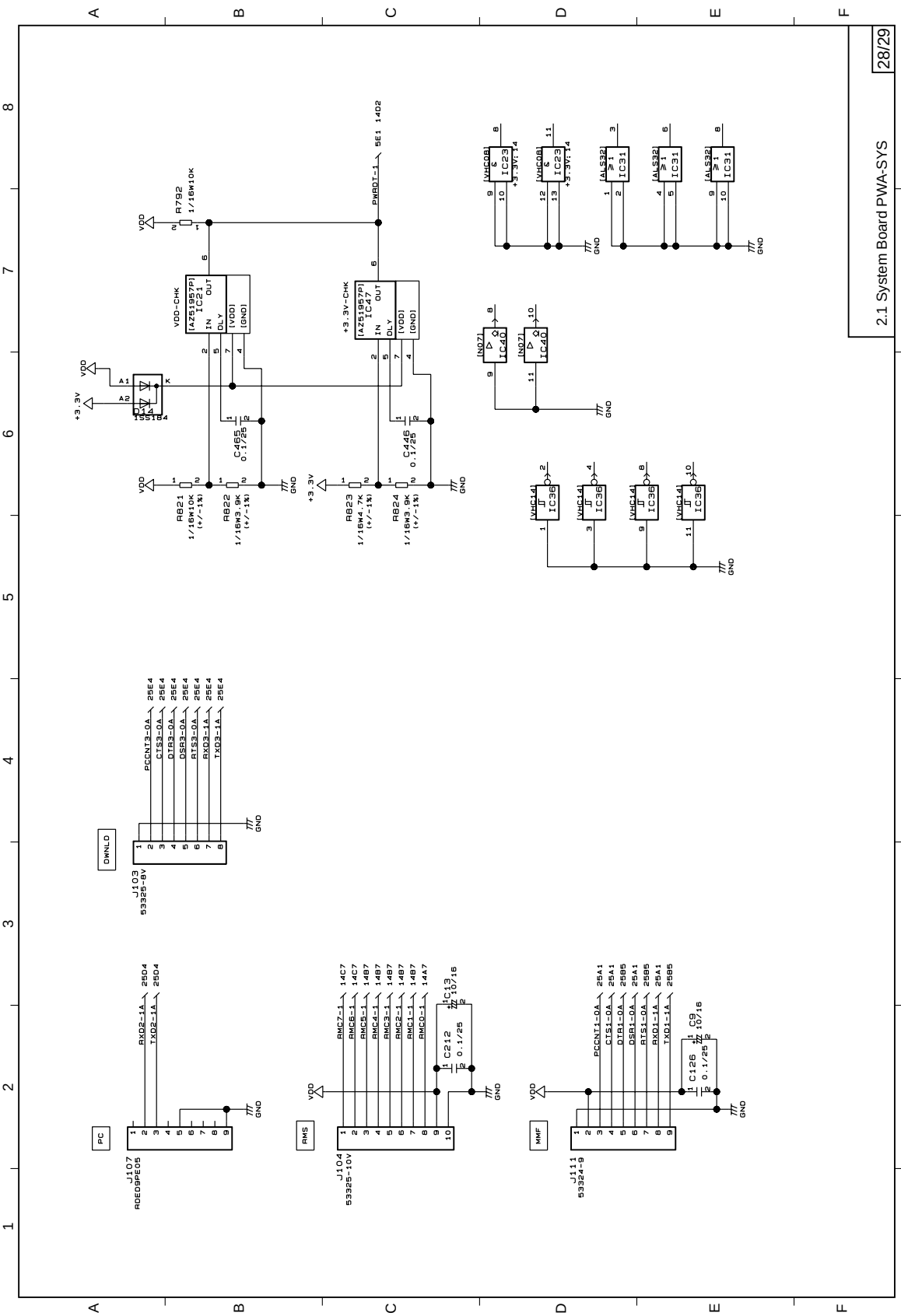

[LGC-I/F]
2.1 System Board PWA-SYS
23/29
SCERR-0
SCACK-0
SSBSY-0
SSIS-1
SCBSY-0A
SSCMD-1A
SSACK-0A
SSERR-0A
SCERR-0A
SCACK-0A
SSBSY-0A
SSIS-1A
SCBSY-0
SSCMD-1
SSACK-0
SSERR-0
13A2
27B8
[未]
IC13
ALS541
R82
1/16W470
GND
VDD
R80 1 2 1/16W22
R99 1 2 1/16W22
R100 1 2 1/16W22
R122 1 2 1/16W22
R106 1 2 1/16W22
R107 1 2 1/16W22
R85 1 2 1/16W22
R84 1 2 1/16W22
R79 1 2 1/16W10K
R97 1 2 1/16W10K
R98 1 2 1/16W10K
R121 1 2 1/16W10K
E53 1 2 0ΩW1/2
E54 1 2 0ΩW1/2
E55 1 2 0ΩW1/2
E56 1 2 0ΩW1/2
E57 1 2 0ΩW1/2
E58 1 2 0ΩW1/2
E59 1 2 0ΩW1/2
E60 1 2 0ΩW1/2
C79 1 2 100P/50
C87 1 2 100P/50
C88 1 2 100P/50
C101 1 2 100P/50
C82 1 2 100P/50
C83 1 2 100P/50
C90 1 2 100P/50
C89 1 2 100P/50
GND

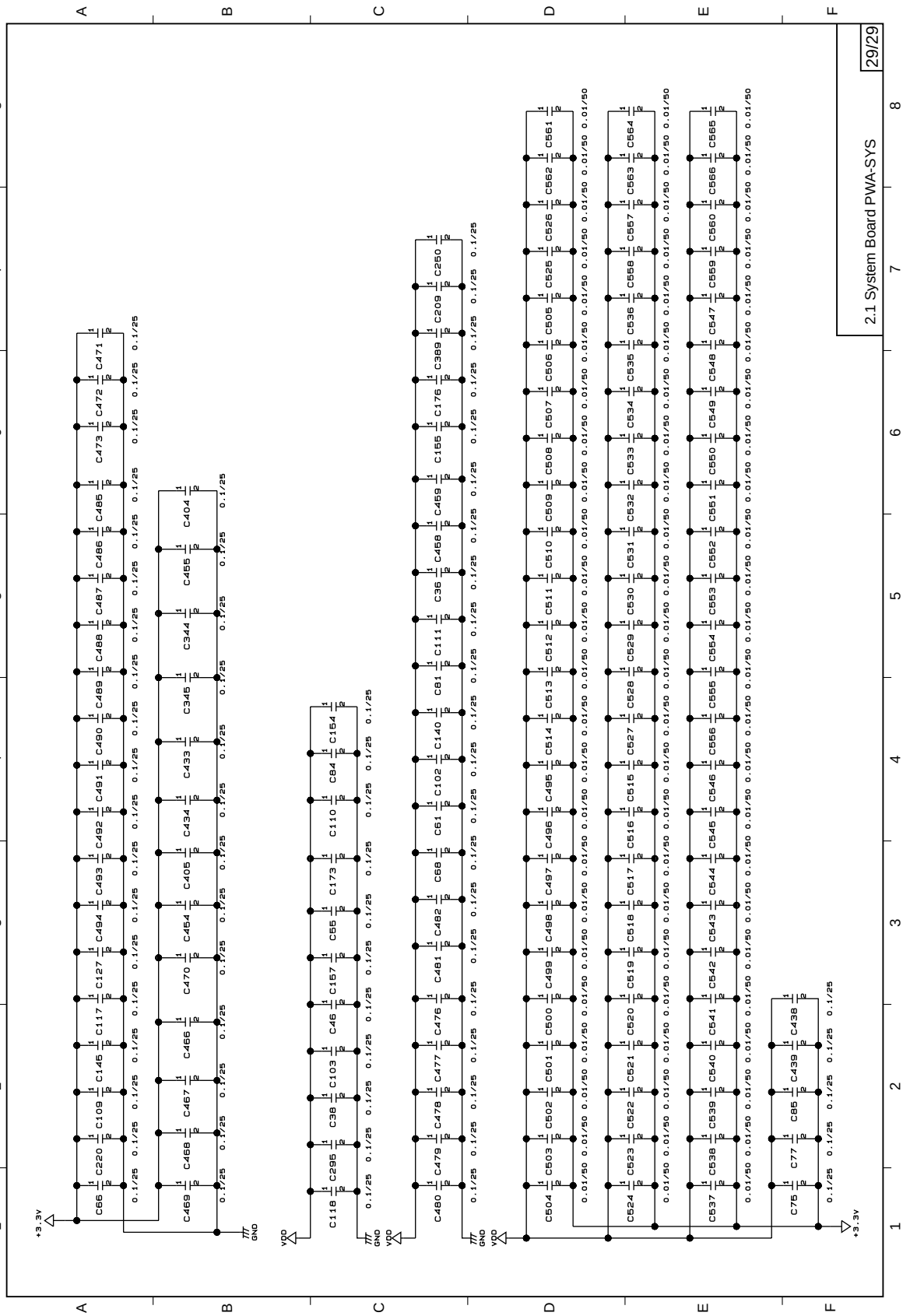

[SLG-I/F]
2.1 System Board PWA-SYS
24/29


2.1 System Board PWA-SYS
25/29
[Down Load]
[未]
[MMF]
RXD
TXD
MSB
LSB
PVDEN
PHDEN
GND
VDD

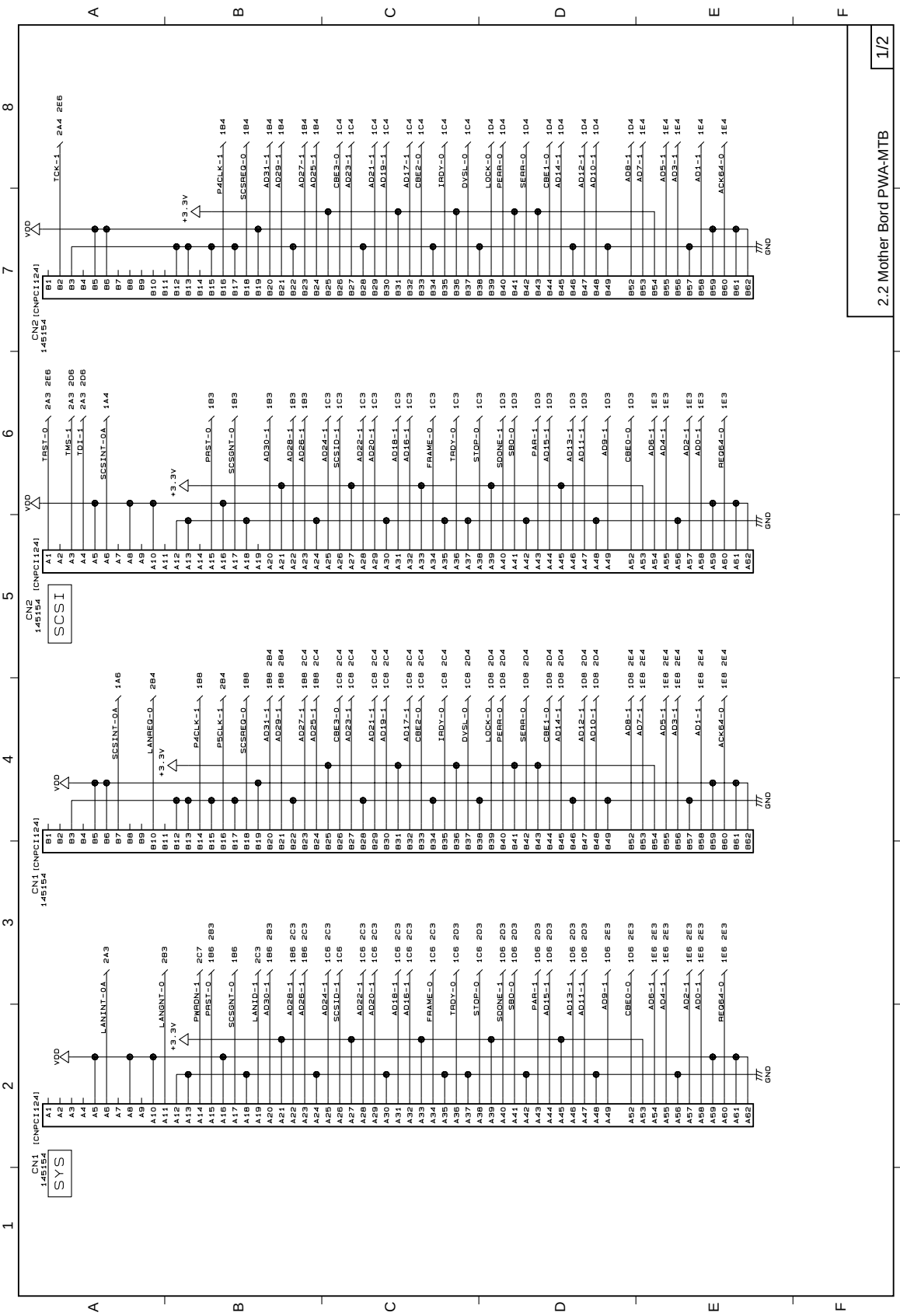

[Card Edge]
SIDE A
SIDE B
2.1 System Board PWA-SYS
26/29
HDD
J106
A3E44PAV
LTI040A
D13
R473
1/10W470
C414
C300
C269
C270
C440
C441
C415
C416
R4021
R3281
R3891
R3271
R3881
R3771
R6491
R2011
R3181
R3171
R3441
R3431
R3121
R3231
+3.3V
VDD
GND
SCSINT-0A
LANREQ-0
SCSREQ-0
LANINT-0A
LANGNT-0
PRST-0
SCSGNT-0
PWRON2-1
PCICLK4
PCICLK5
IDRST-0A
IDREQ-1A
DIOWR-0A
DIORD-0A
IOCRDY-1A
IOACK-0A
HIREQ-1A
ADR1-1A
ADR0-1A
ADR2-1A
CSA0-0A
CSA1-0A
HDDRV
DATA7-1A
DATA6-1A
DATA5-1A
DATA4-1A
DATA3-1A
DATA2-1A
DATA1-1A
DATA0-1A
DATA15-1A
DATA14-1A
DATA13-1A
DATA12-1A
DATA11-1A
DATA10-1A
DATA9-1A
DATA8-1A
AD31-1
AD29-1
AD27-1
AD25-1
CBE3-0
AD23-1
AD21-1
AD19-1
AD17-1
CBE2-0
IRDY-0
DVSL-0
LOCK-0
PERR-0
SERR-0
CBE1-0
AD14-1
AD12-1
AD10-1
AD8-1
AD7-1
AD5-1
AD3-1
AD1-1
ACK64-0
AD22-1
AD20-1
AD18-1
AD16-1
FRAME-0
TRDY-0
STOP-0
SDONE-1
SB0-0
PAR-1
AD15-1
AD13-1
AD11-1
AD9-1
CBE0-0
AD6-1
AD4-1
AD2-1
AD0-1
REQ64-0
AD24-1
SCSIO-1
AD26-1
AD28-1
LANIO-1
AD30-1
2/10K1K LANREQ-0
2/10K1K SCSREQ-0
2/10K1K PERR-0
2/10K1K SERR-0
2/10K1K SDONE-1
2/10K1K SB0-0
2/10K1K REQ64-0
2/10K1K ACK64-0
2/10K1K FRAME-0
2/10K1K IRDY-0
2/10K1K TRDY-0
2/10K1K DVSL-0
2/10K1K STOP-0
2/10K1K LOCK-0
[未]
100P/50
1/16SM100
0.1/25
10/16
100/16
CARDEDGE

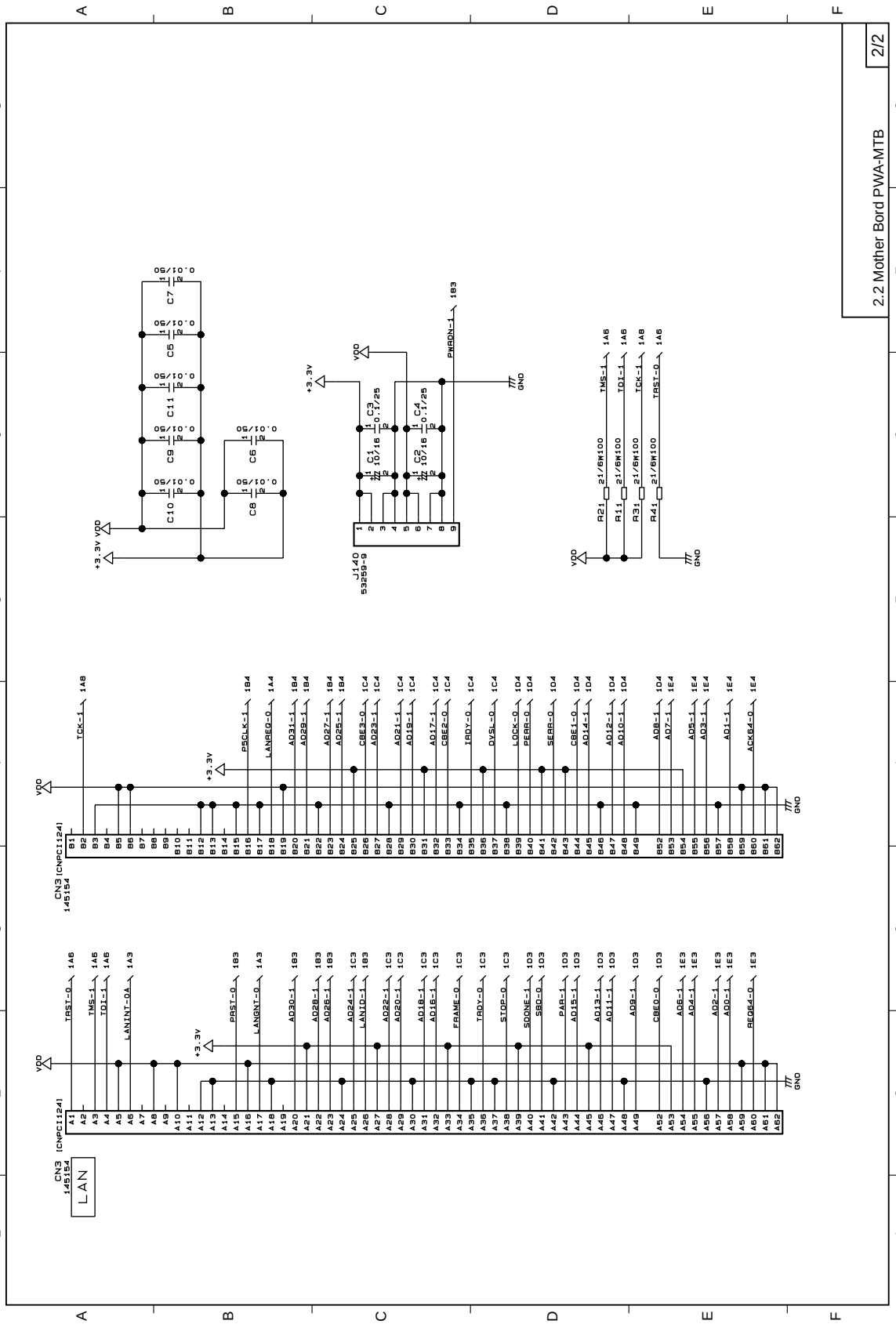

2.1 System Board PWA-SYS
27/29
LGC
PLG
SLG
FAN
PANEL
POWER
J102
J109
J108
J110
J105
J101
Q2
Q3
D1
D2
R503
R232
R681
R2681
C213
C222
C35
C80
C1
C5
C14
C15
TP75
TP76
TP77
GND
VDD
+3.3V
+5V


2.1 System Board PWA-SYS
28/29
PWRBDT-1
VDD-CHK
+3.3V-CHK
R792
1/16W10K
C465
0.1/25
C446
0.1/25
R821
1/16W10K (+/-1%)
R822
1/16W3.9K (+/-1%)
R823
1/16W4.7K (+/-1%)
R824
1/16W3.9K (+/-1%)
D14
1SS184
J103
53325-8V
DWNLD
PCCNT3-0A
CTS3-0A
DTR3-0A
DSR3-0A
RTS3-0A
RXD3-1A
TXD3-1A
J107
RDE09PE05
PC
RXD2-1A
TXD2-1A
J104
53325-10V
RMS
C212
0.1/25
C13
10/16
J111
53324-9
MMF
C126
0.1/25
C9
10/16
IC23
IC31
IC36
IC40
GND
VDD
+3.3V

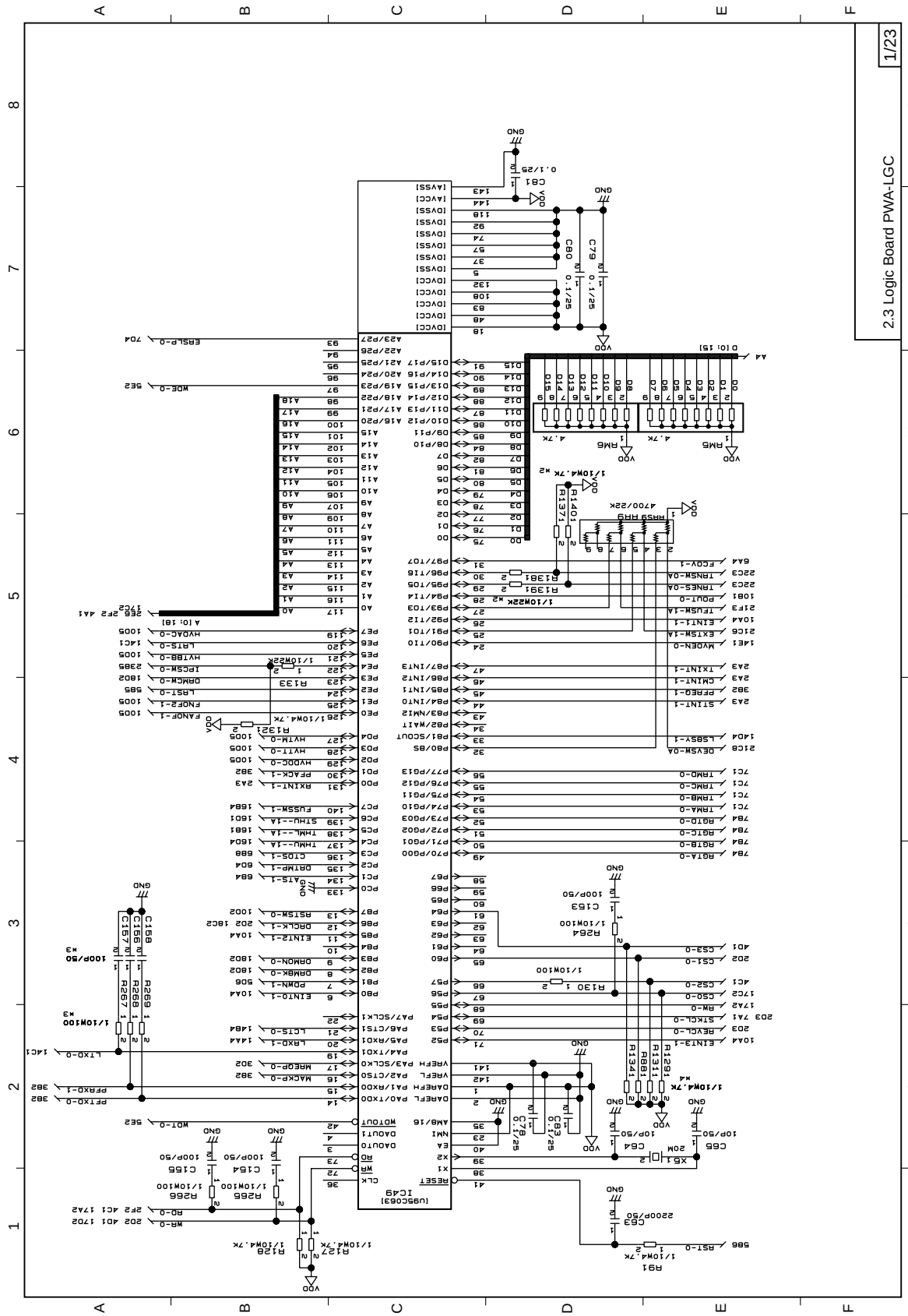

2.1 System Board PWA-SYS
29/29

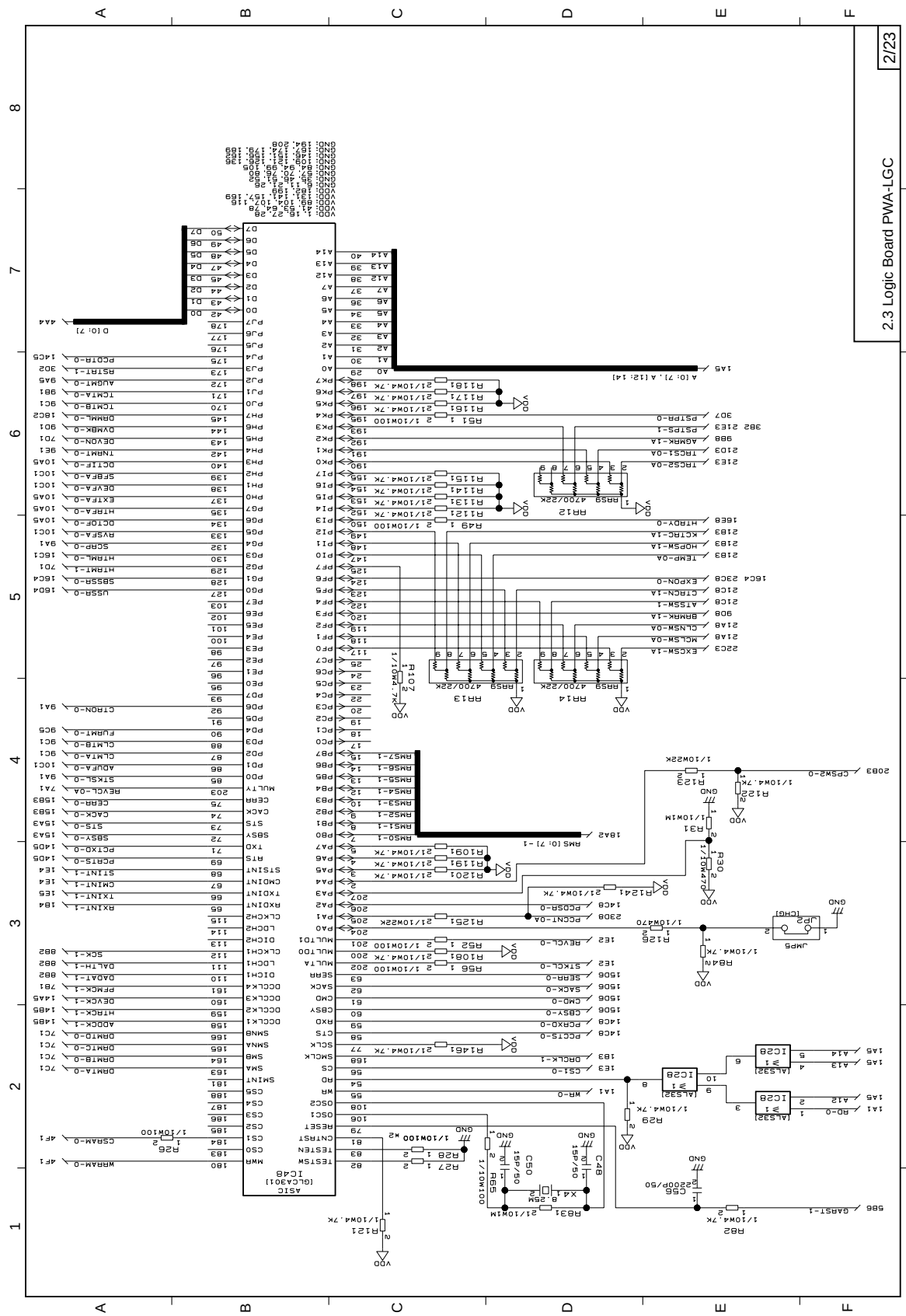
2.2 Mother Board (PWA-MTB) 1/2~2/2

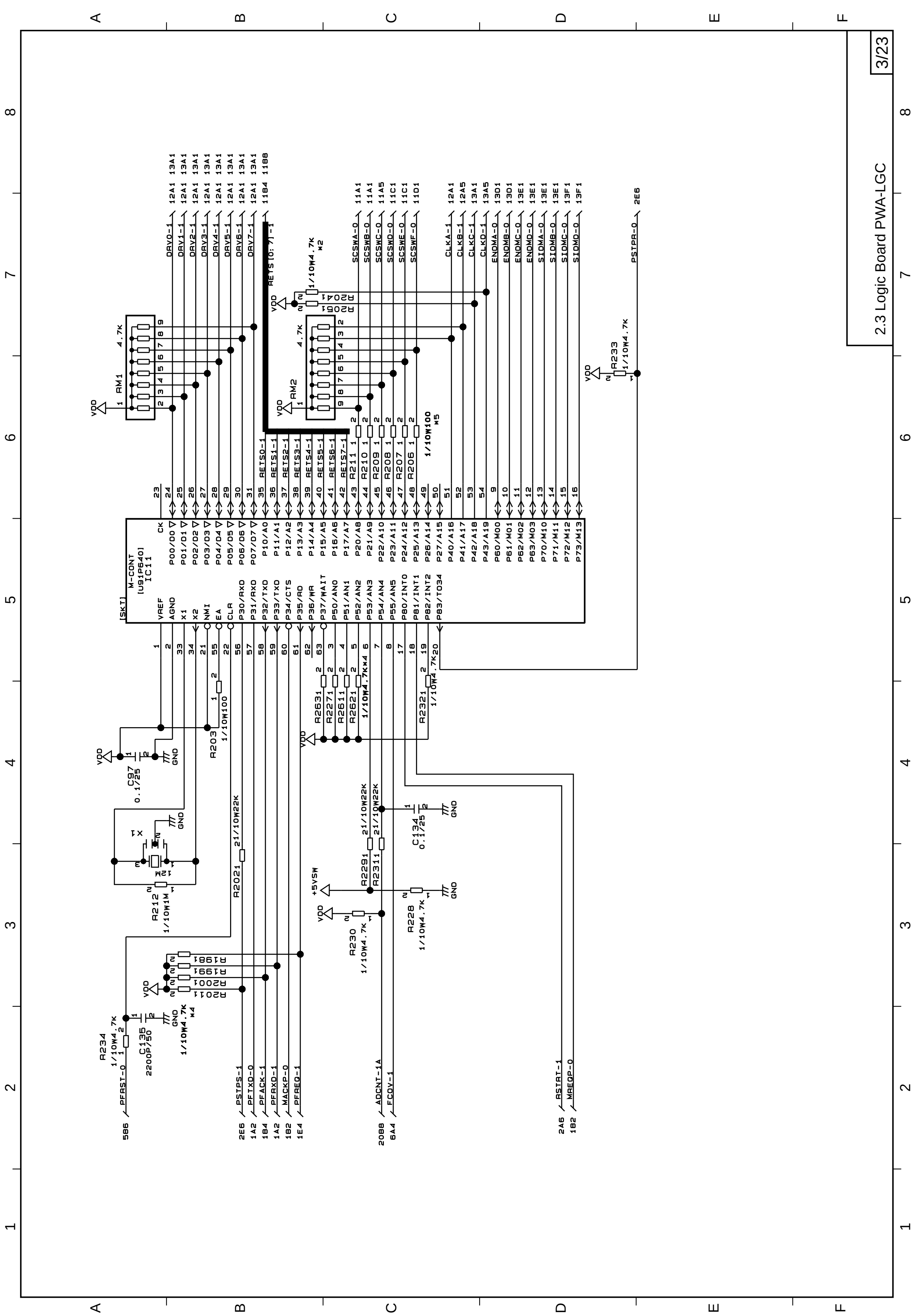


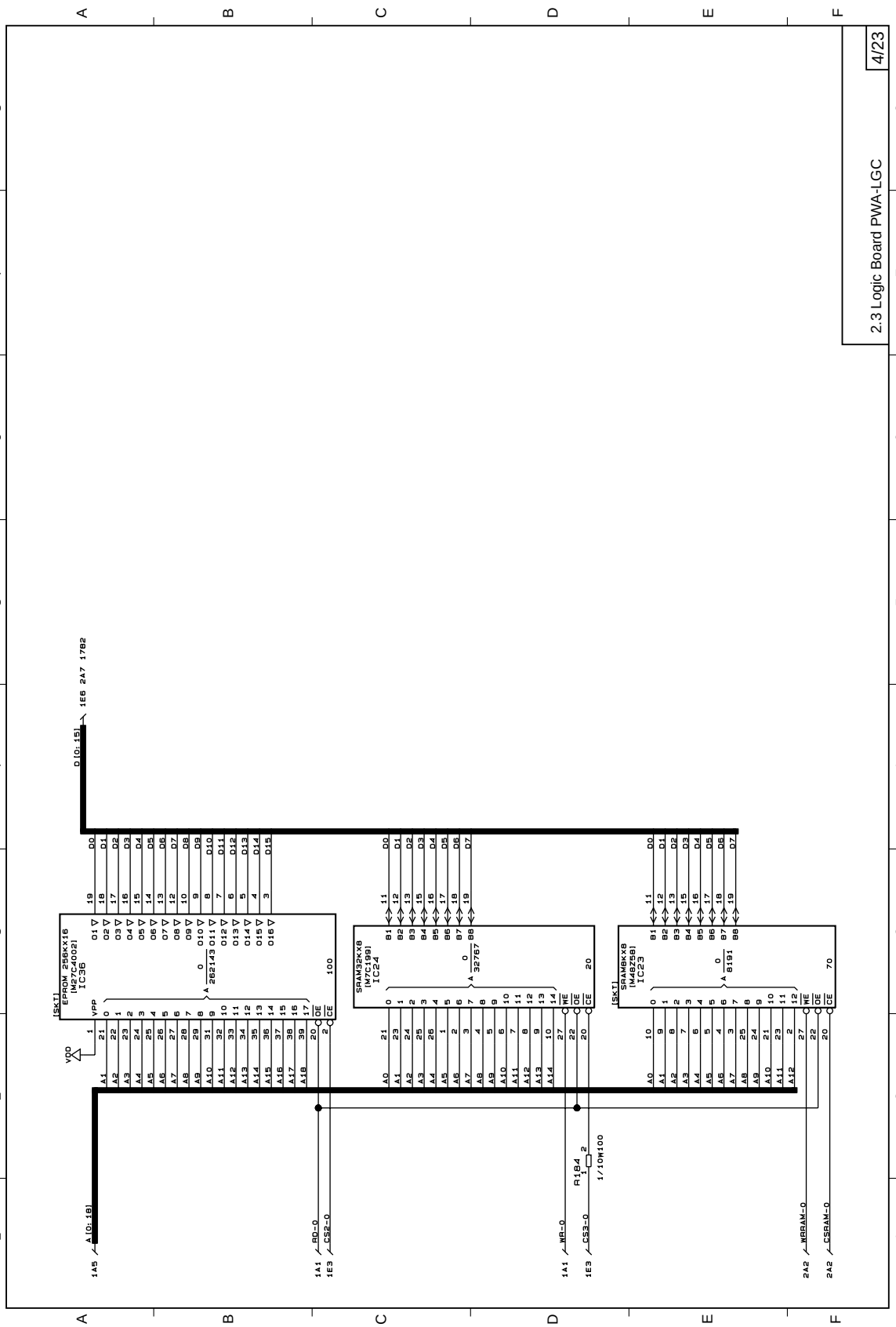

2.2 Mother Bord PWA-MTB
2/2
LAN

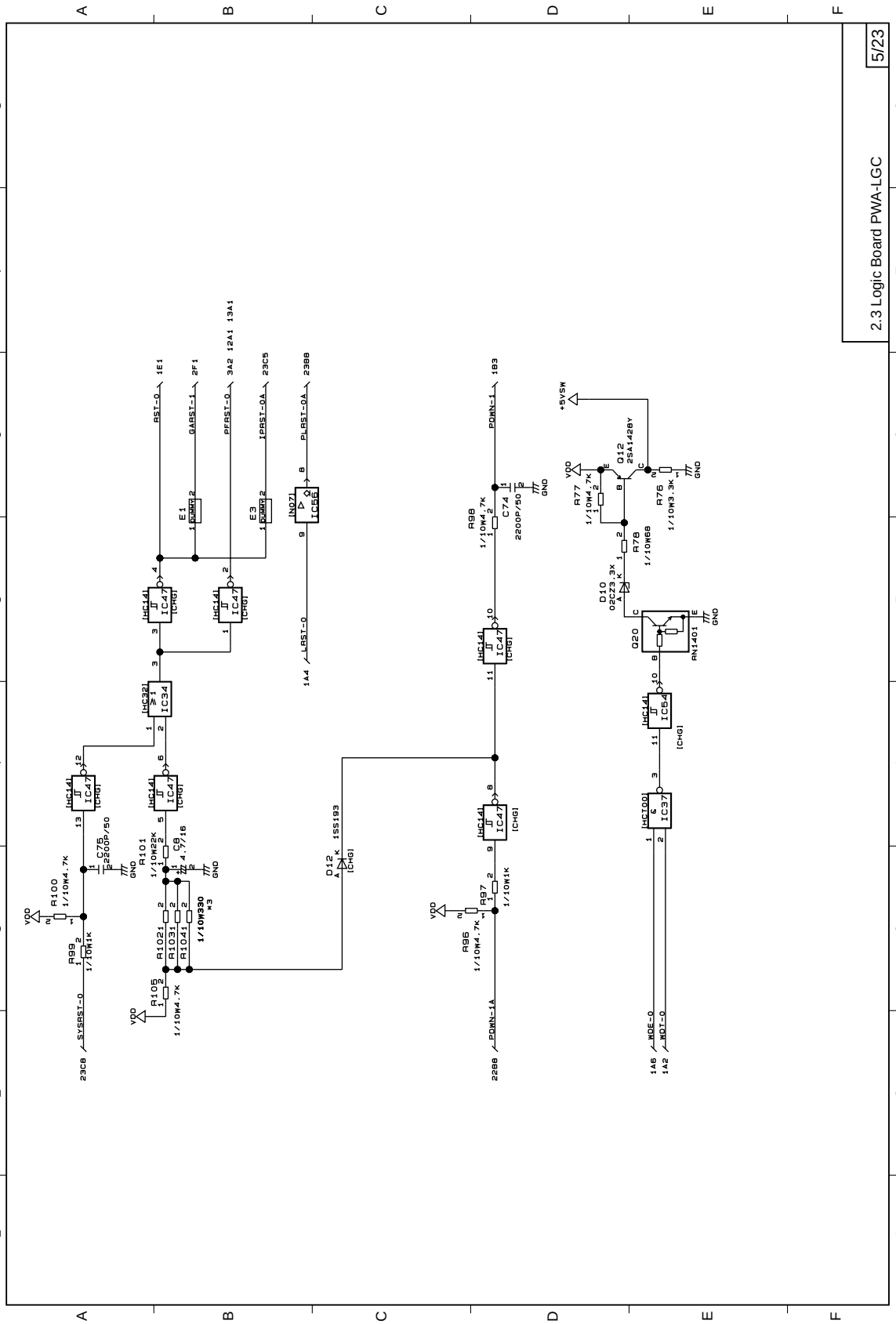
2.3 Logic Board (PWA-LGC) 1/23~23/23

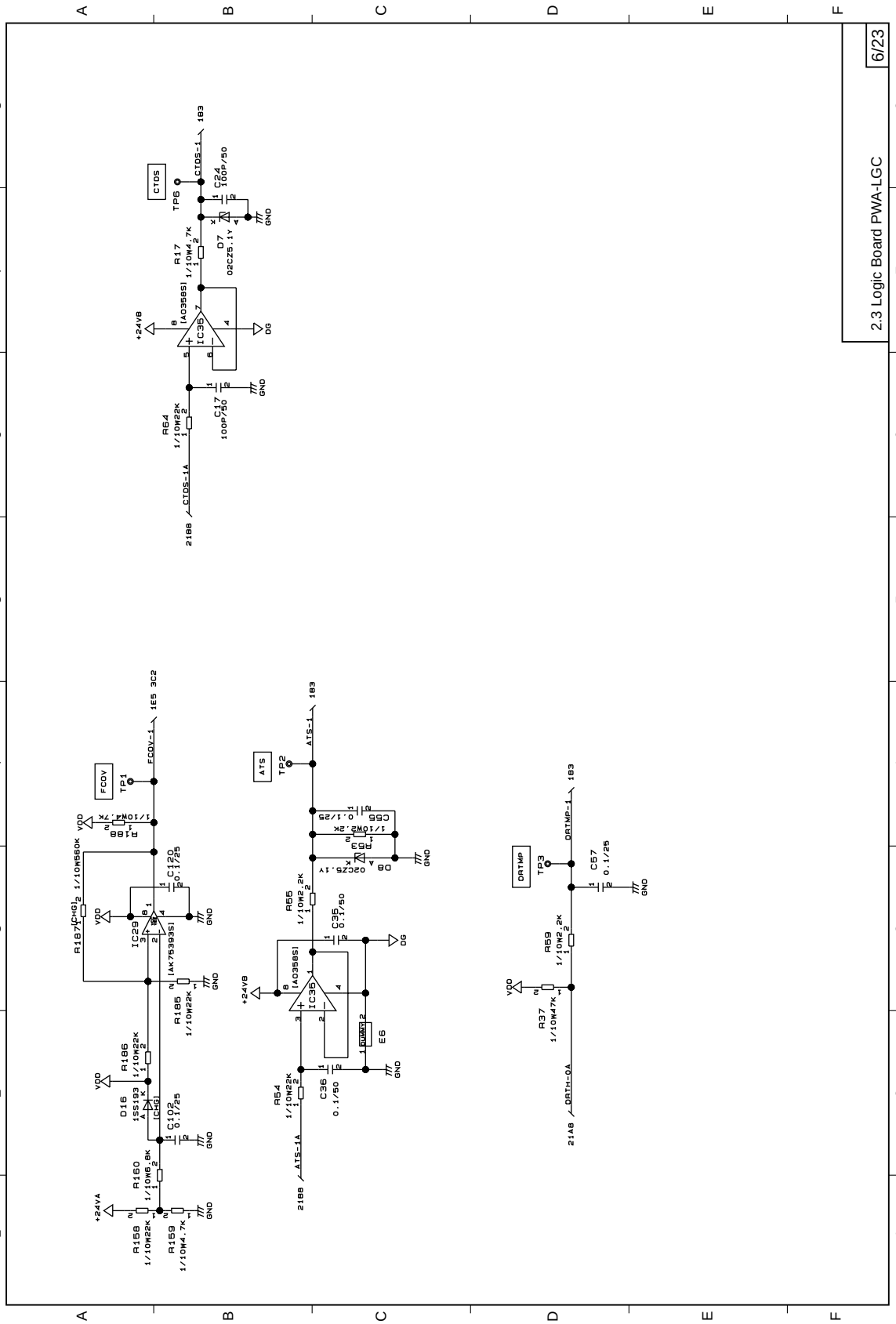


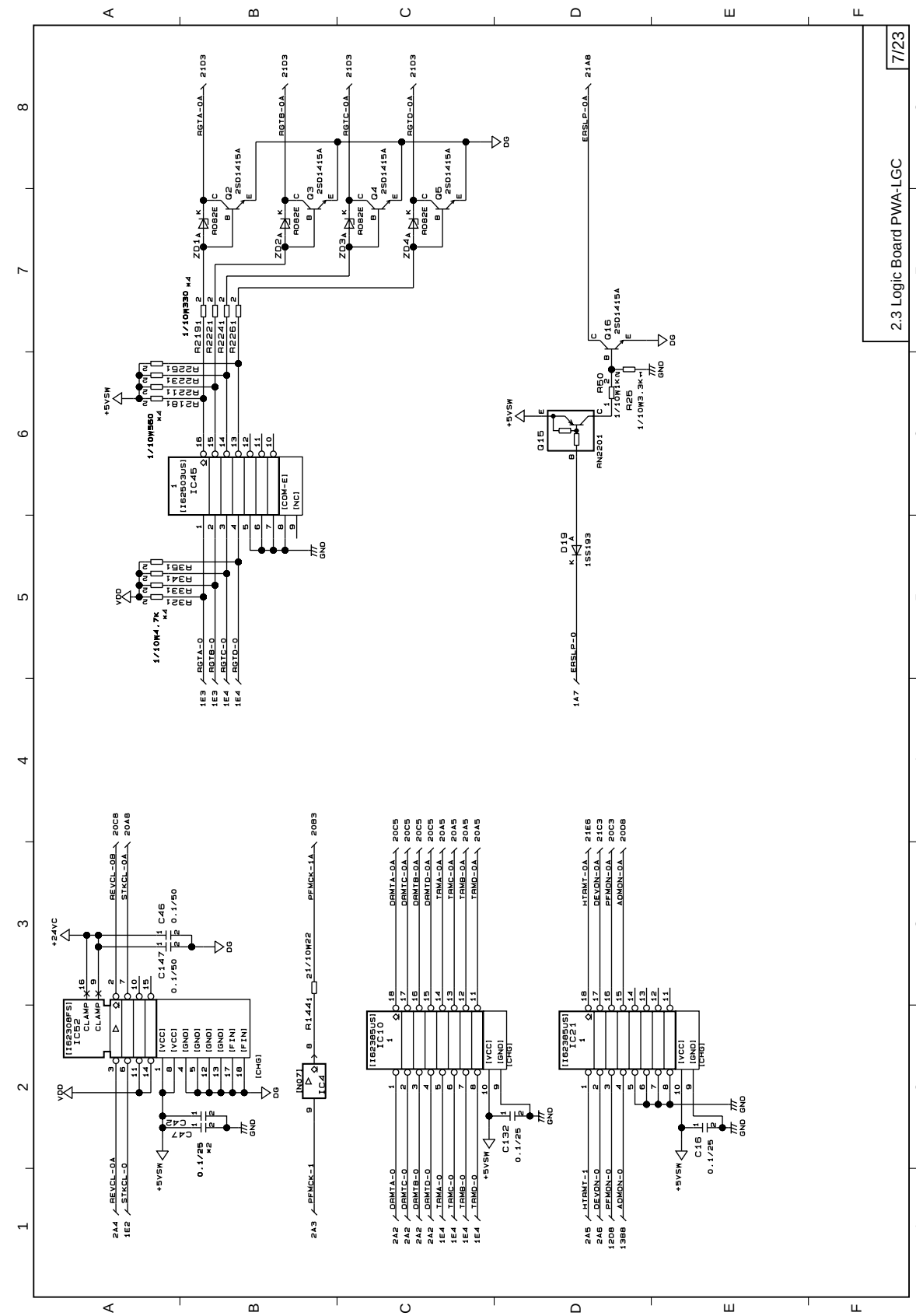

2/23
2.3 Logic Board PWA-LGC
ASIC
IC48
(GLCA301)

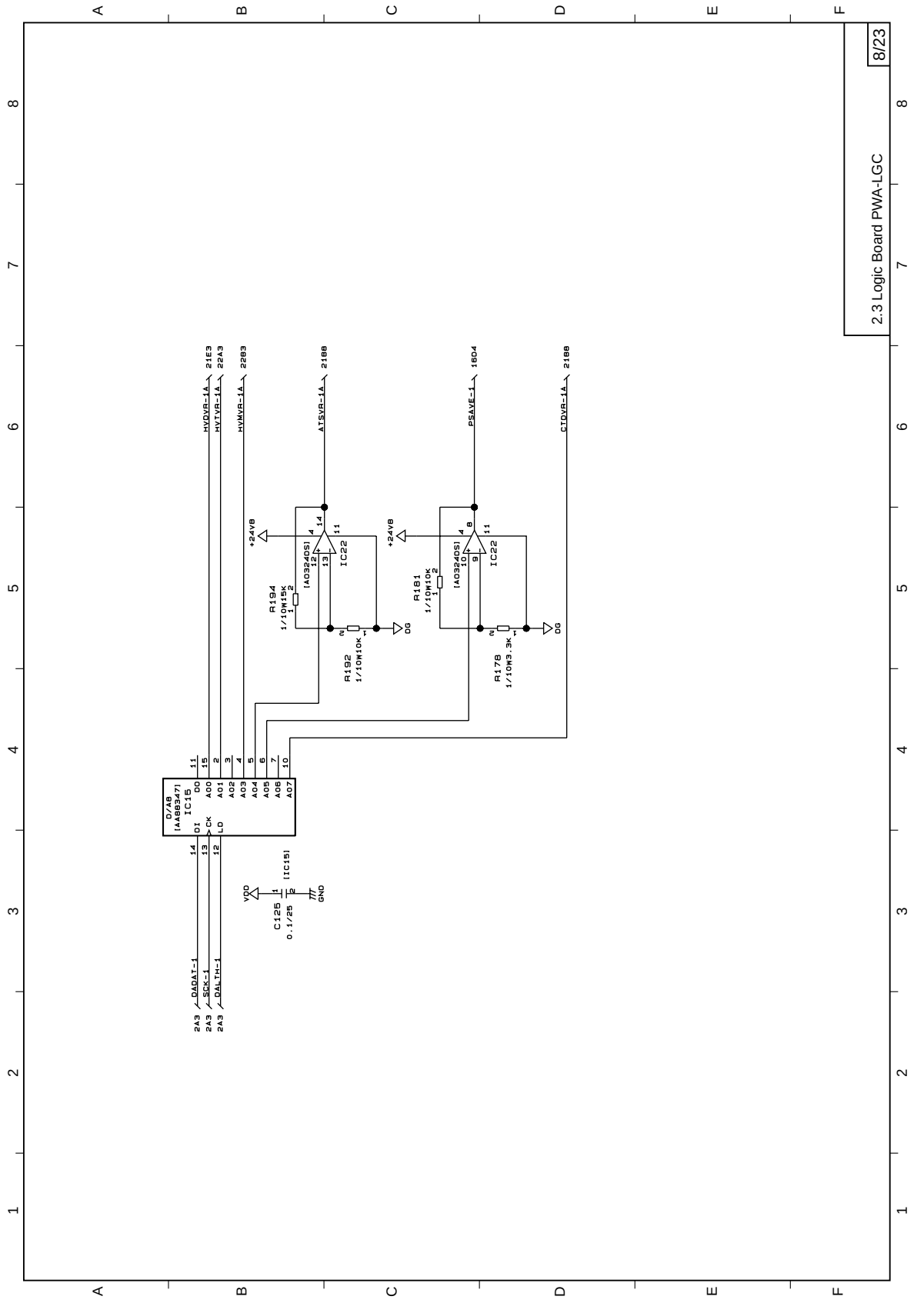

2.3 Logic Board PWA-LGC
3/23
M-CONT
(U91P640)
IC11

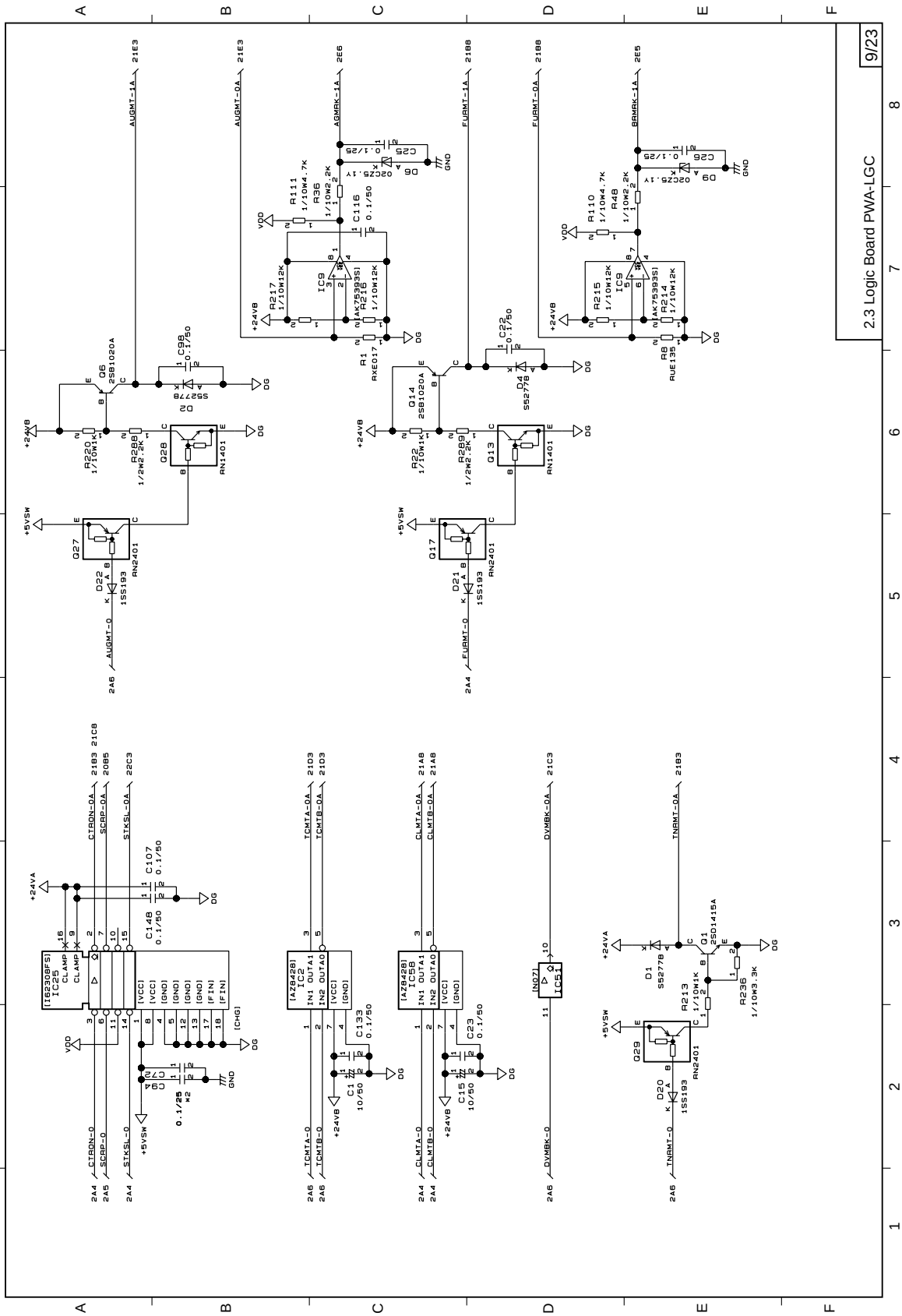

2.3 Logic Board PWA-LGC
4/23
EPROM 256Kx16
IM27C4002
IC36
SRAM32Kx8
IM7C199I
IC24
SRAM8Kx8
IM48Z58I
IC23
R184
1/10W100
D[0:15]
A[0:18]
RD-0
CS2-0
WR-0
CS3-0
WRRAM-0
CSRAM-0

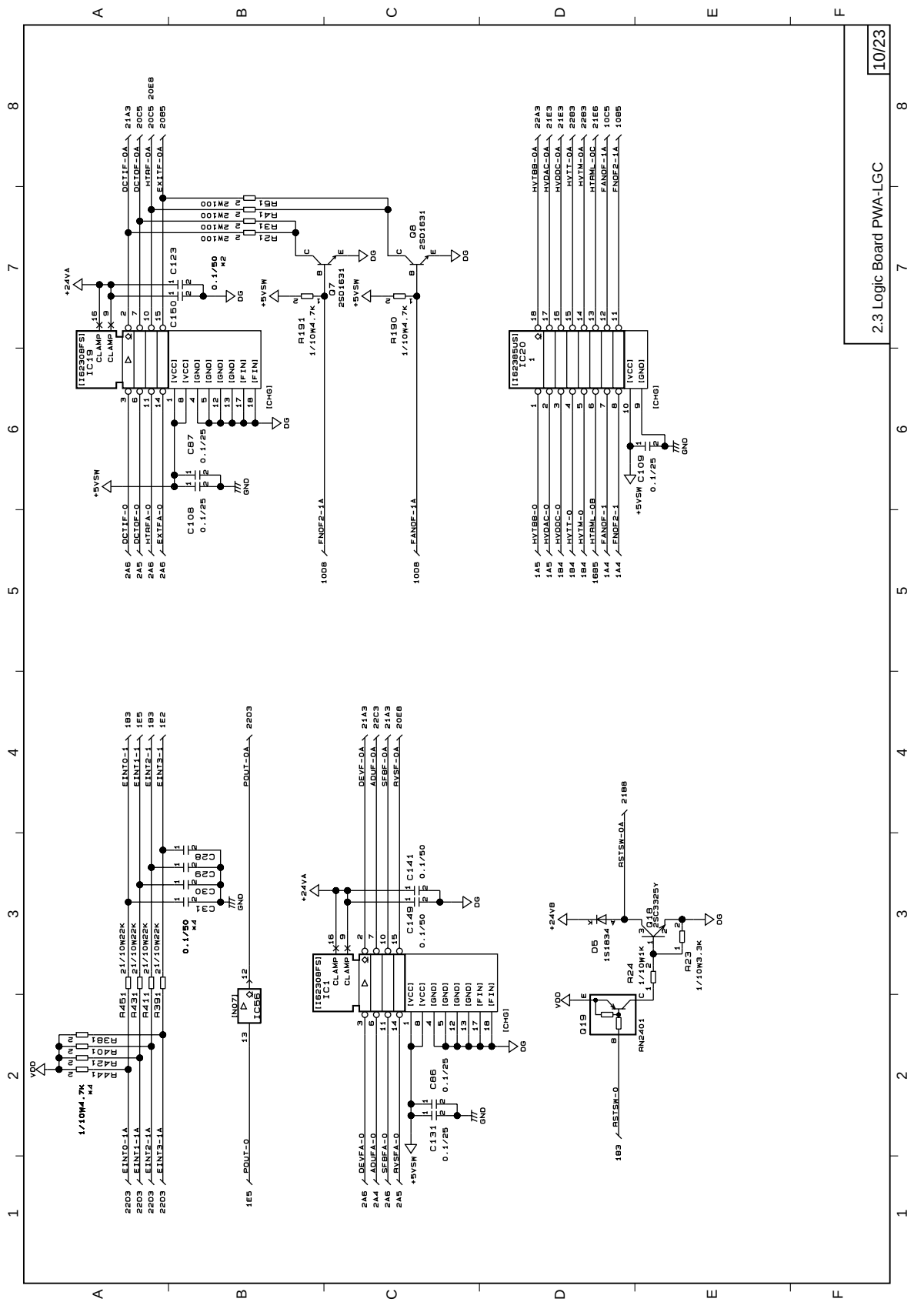

2.3 Logic Board PWA-LGC
5/23

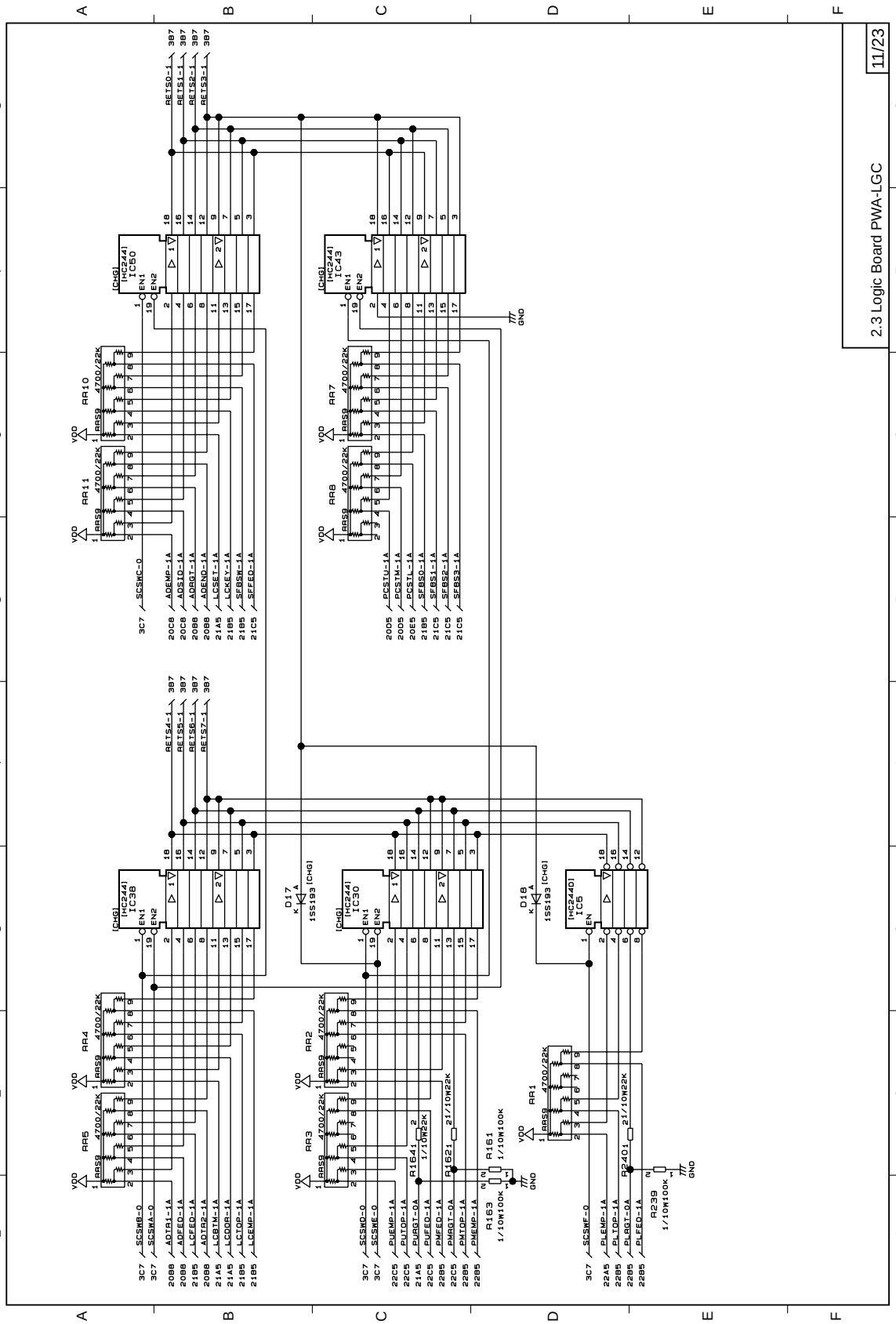

2.3 Logic Board PWA-LGC
6/23
CTOS
TP6
CTOS-1
C24
100P/50
D7
02CZ5.1V
R17
1/10W4.7K
IC35
BA03585
+24VB
DG
R64
1/10W22K
C17
100P/50
GND
2188
CTOS-1A
ATS
TP2
ATS-1
C55
0.1/25
R53
1/10W2.2K
D8
02CZ5.1V
R55
1/10W2.2K
C35
0.1/50
IC36
BA03585
E6
R54
1/10W22K
C36
0.1/50
ATS-1A
FCOV
TP1
FCOV-1
R188
1/10W4.7K
VDD
C120
0.1/25
R187
1/10W560K
IC29
AK7533SI
R185
1/10W22K
R186
1/10W22K
D16
1SS193
C102
0.1/25
R160
1/10W8.2K
R158
1/10W22K
R159
1/10W4.7K
+24VA
DRTMP
TP3
DRTMP-1
C57
0.1/25
R69
1/10W2.2K
R37
1/10W47K
DRTH-0A
2148
1E5 3C2
183
GND
DG

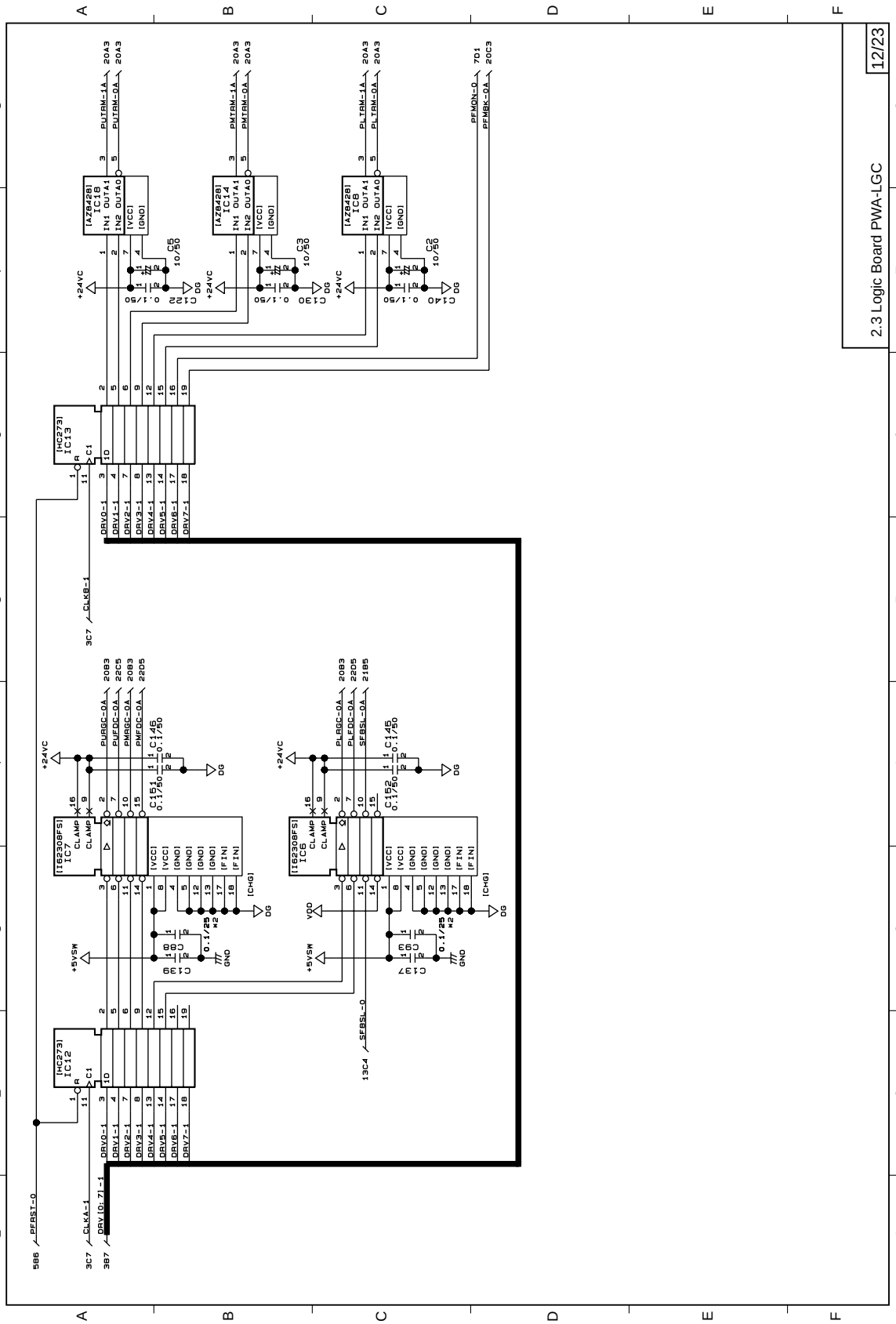

2.3 Logic Board PWA-LGC
7/23

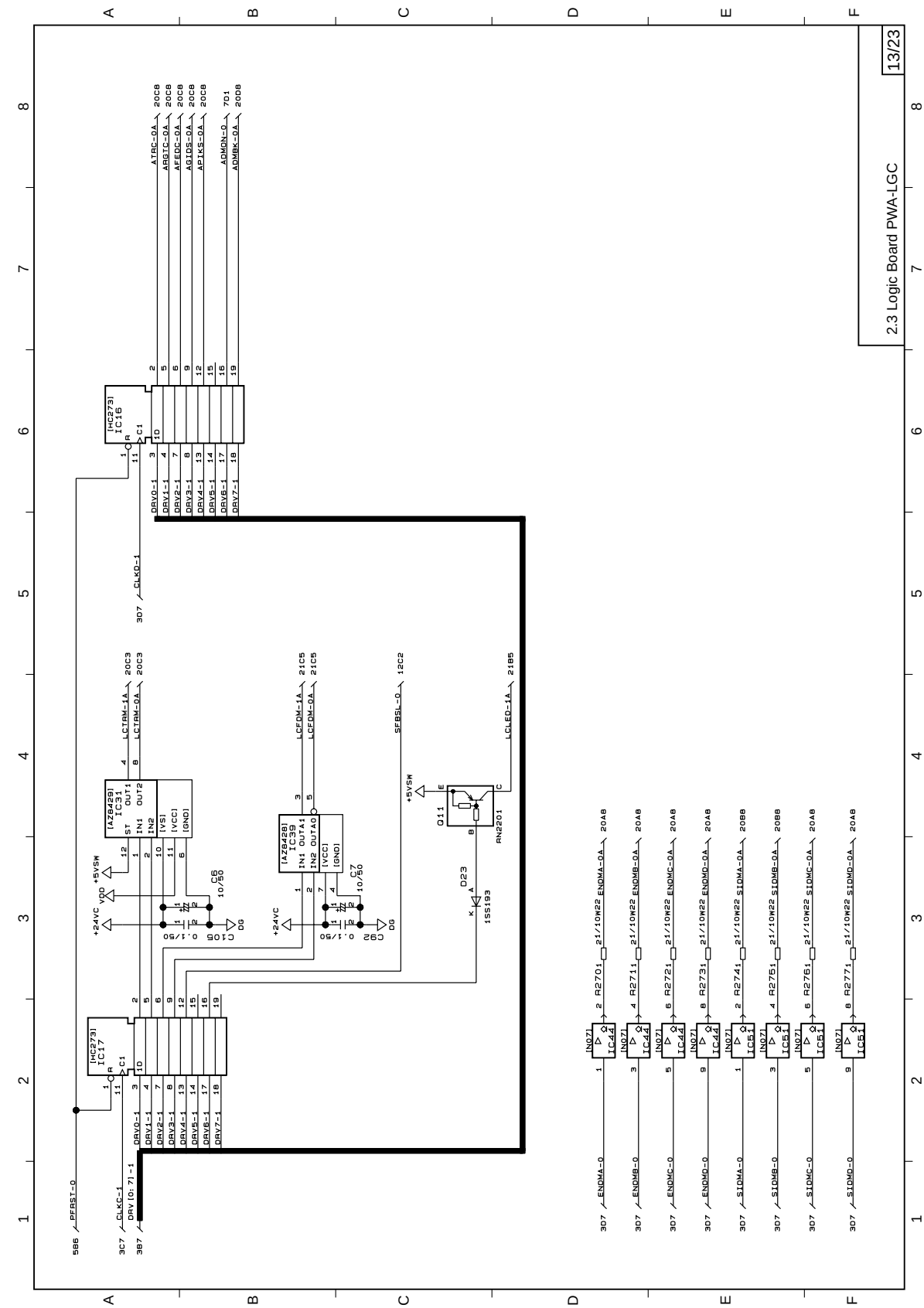

2.3 Logic Board PWA-LGC
8/23
D/AB
[AA883471
IC15
DI
CK
LD
DO
A00
A01
A02
A03
A04
A05
A06
A07
DADAT-1
SCK-1
DALTH-1
VDD
GND
C125
0.1/25
[IC15]
R194
1/10W15K
R192
1/10W10K
R181
1/10W10K
R178
1/10W3.3K
[AO3240S]
IC22
+24VB
DG
HVDVR-1A
HVIVR-1A
HVMVR-1A
ATSVR-1A
PSAVE-1
CIDVR-1A

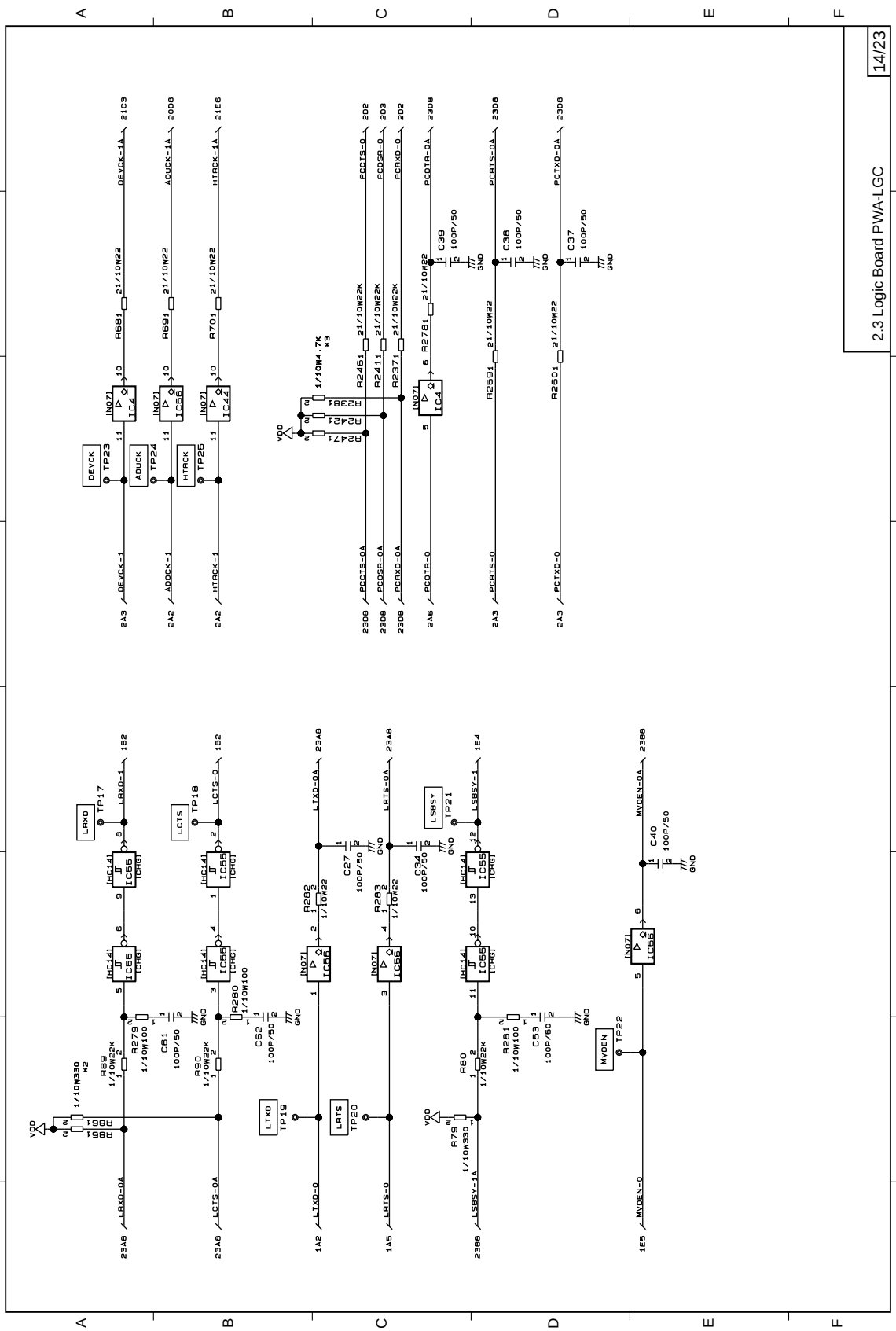

2.3 Logic Board PWA-LGC
9/23

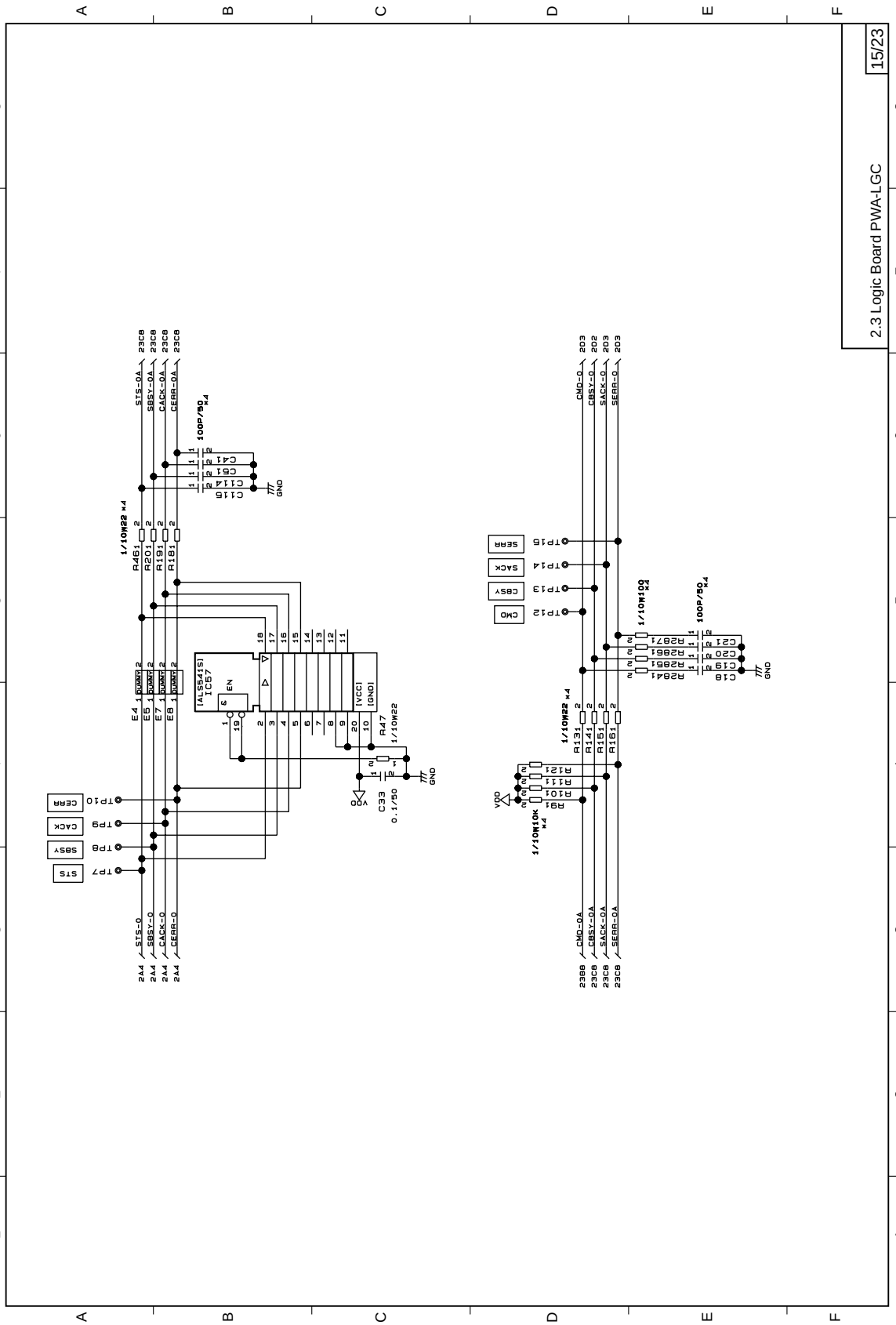

2.3 Logic Board PWA-LGC
10/23

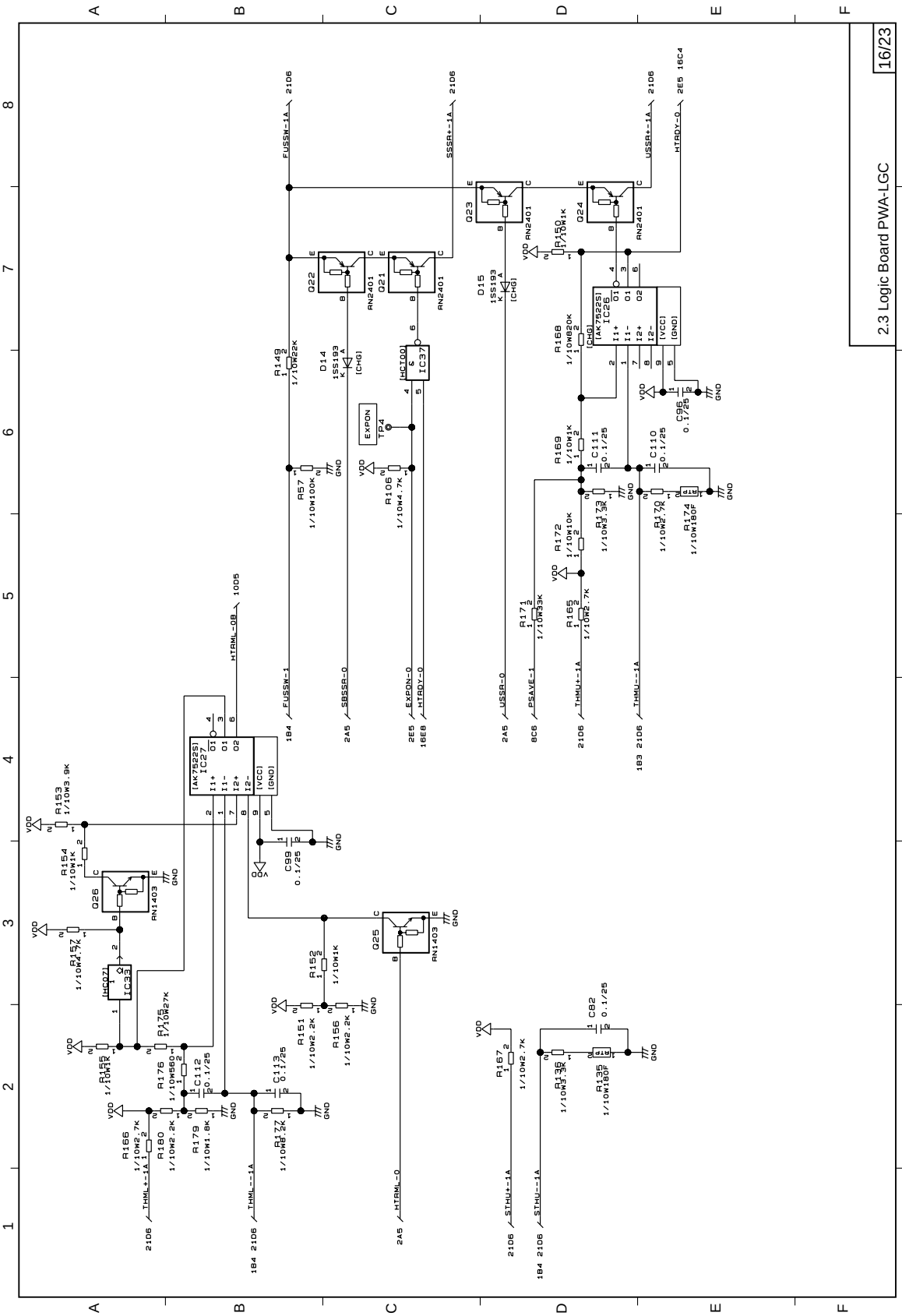

2.3 Logic Board PWA-LGC
11/23

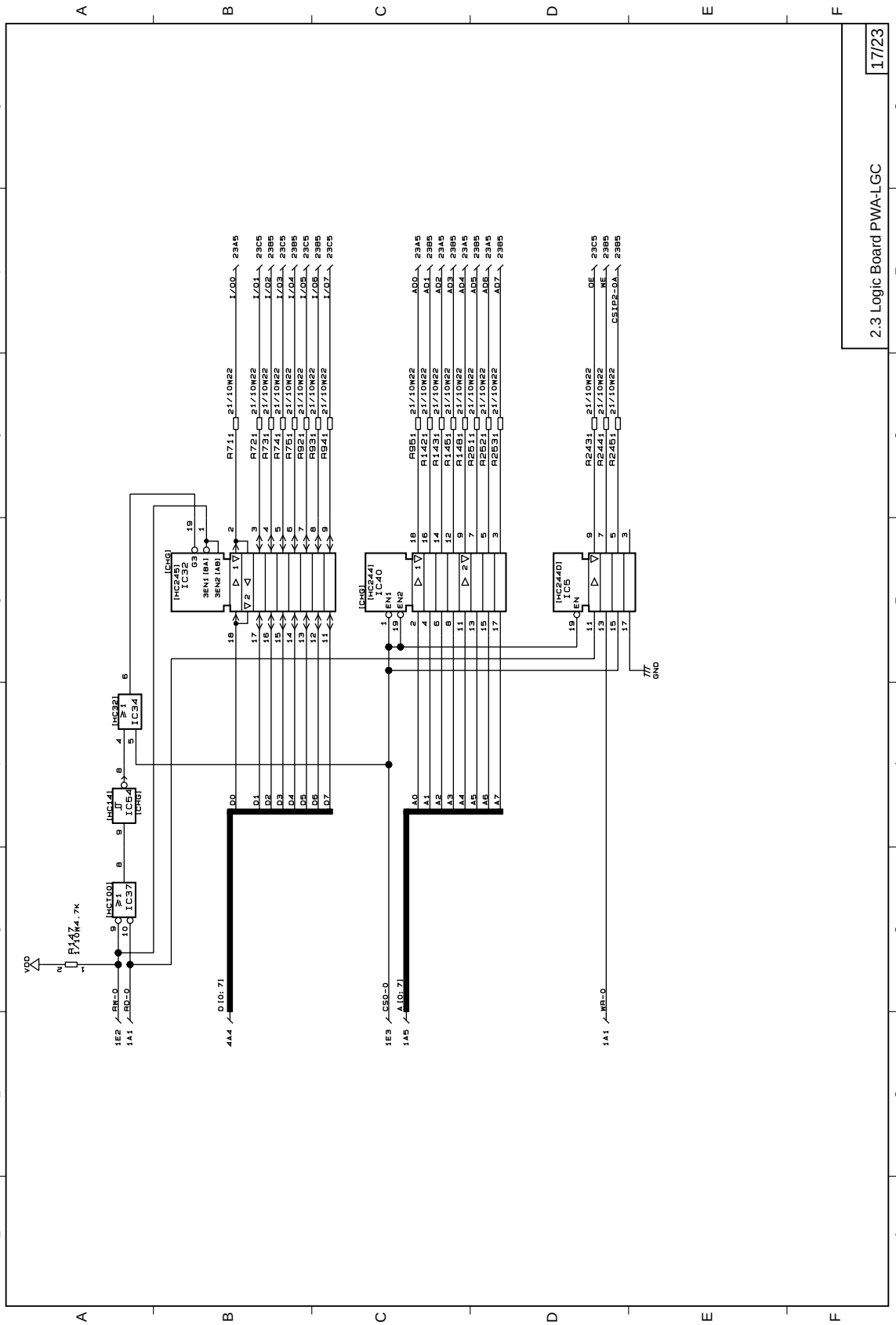

2.3 Logic Board PWA-LGC
12/23

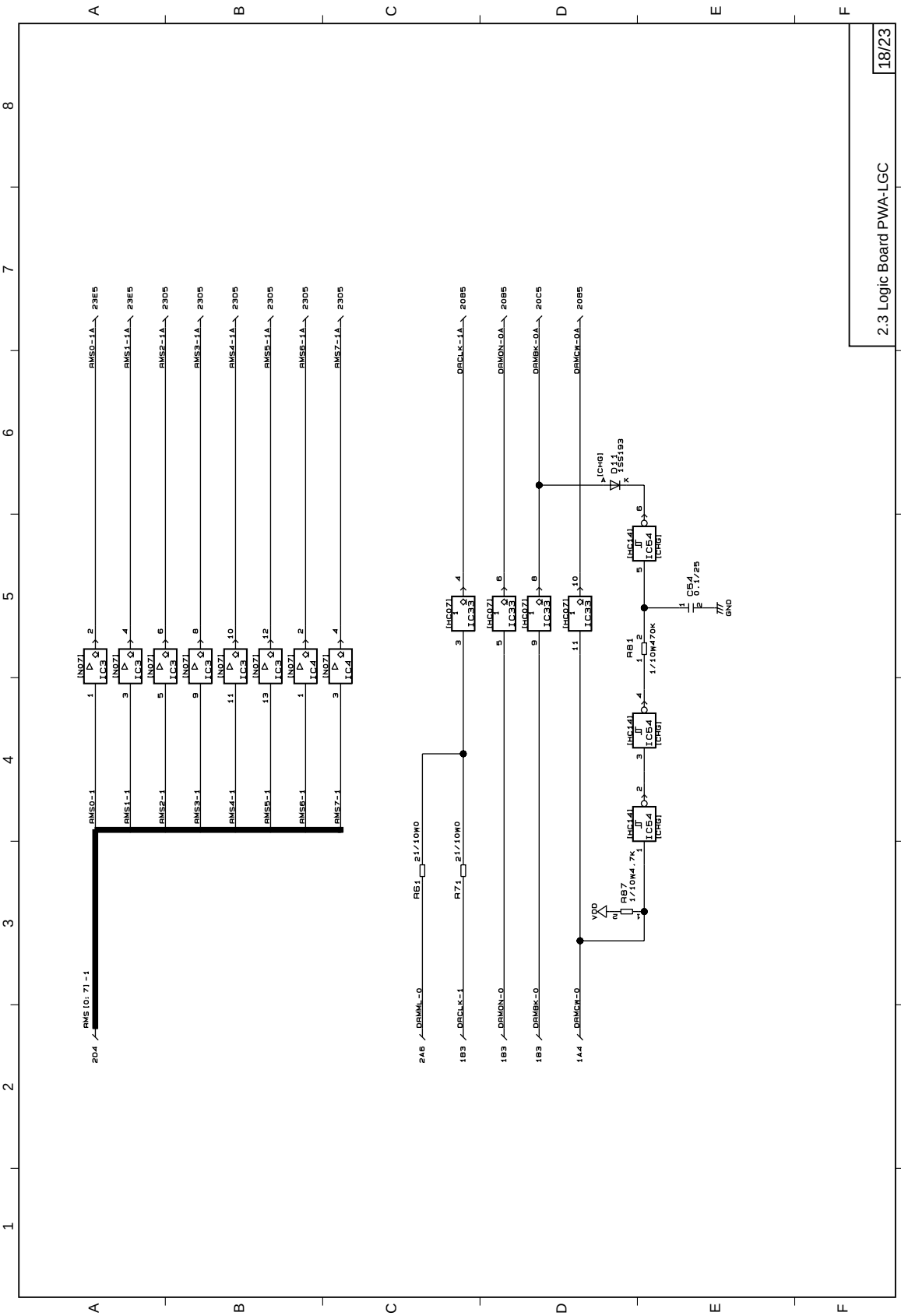

2.3 Logic Board PWA-LGC
13/23

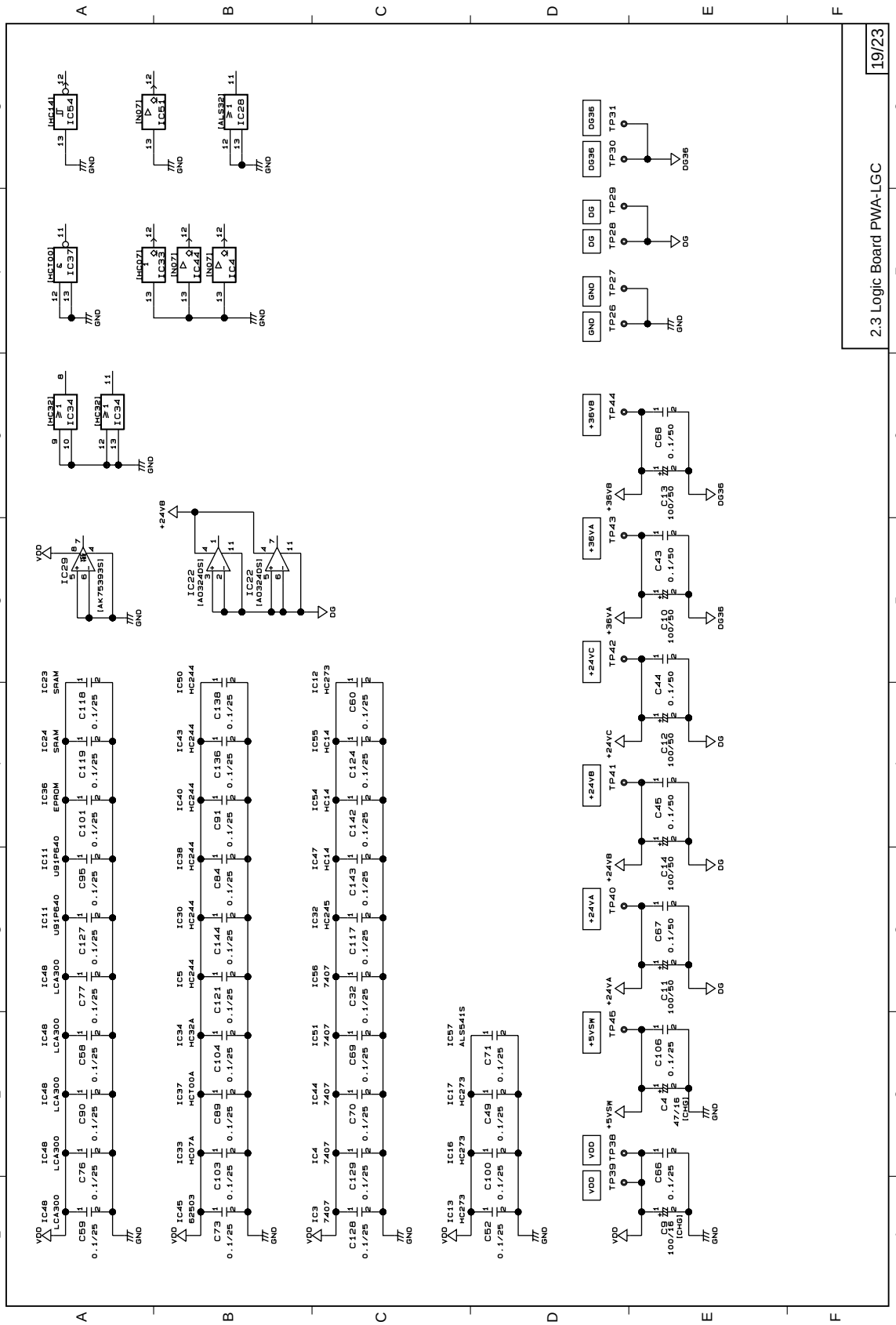

2.3 Logic Board PWA-LGC
14/23

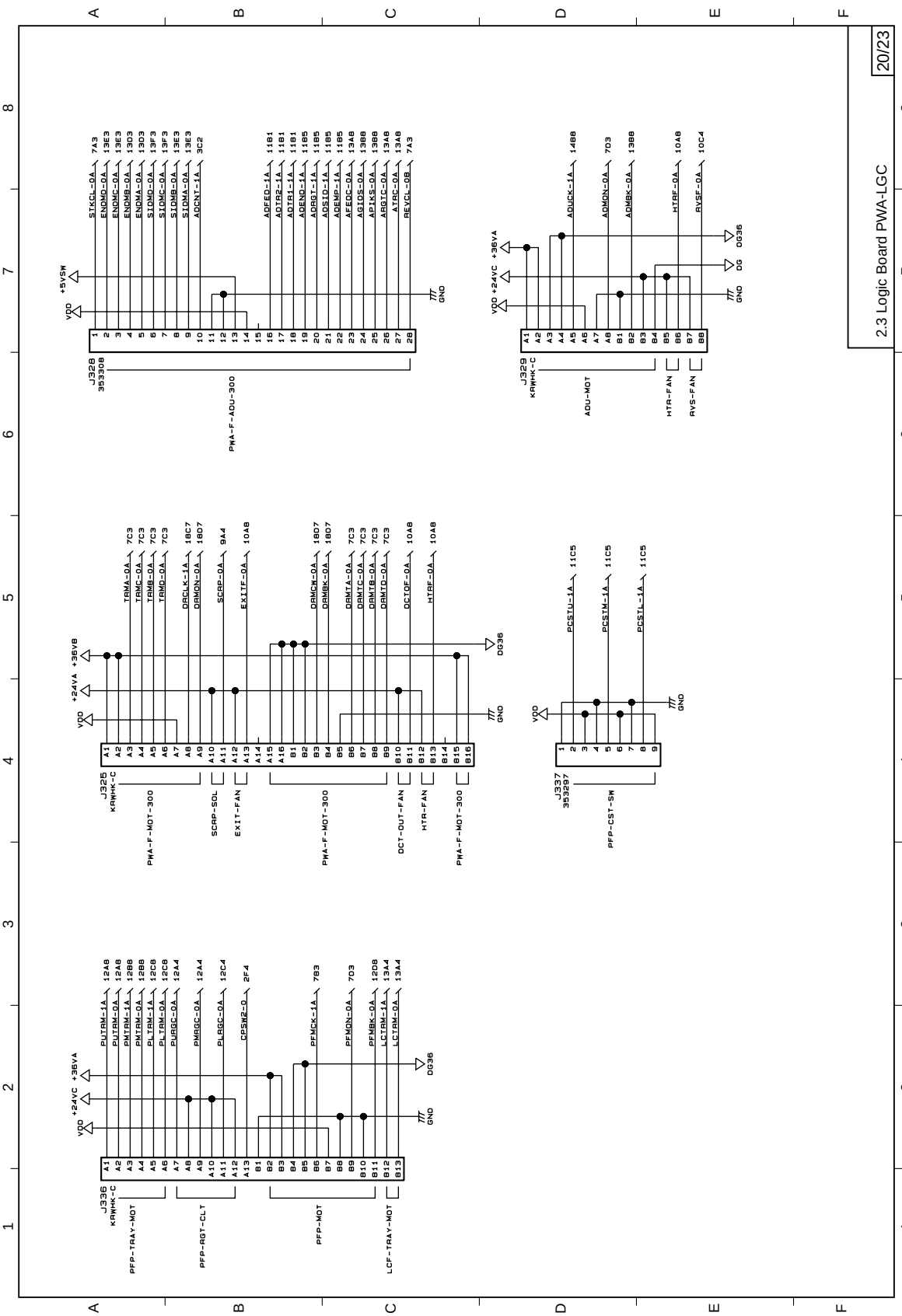

2.3 Logic Board PWA-LGC
15/23
STS
SBSY
CACK
CERR
SERR
CBSY
SACK
CMD
[ALS541S]
1/10W22
1/10W100
1/10K10
100P/50
0.1/50
GND
VDD
[VCC]
[GND]
EN

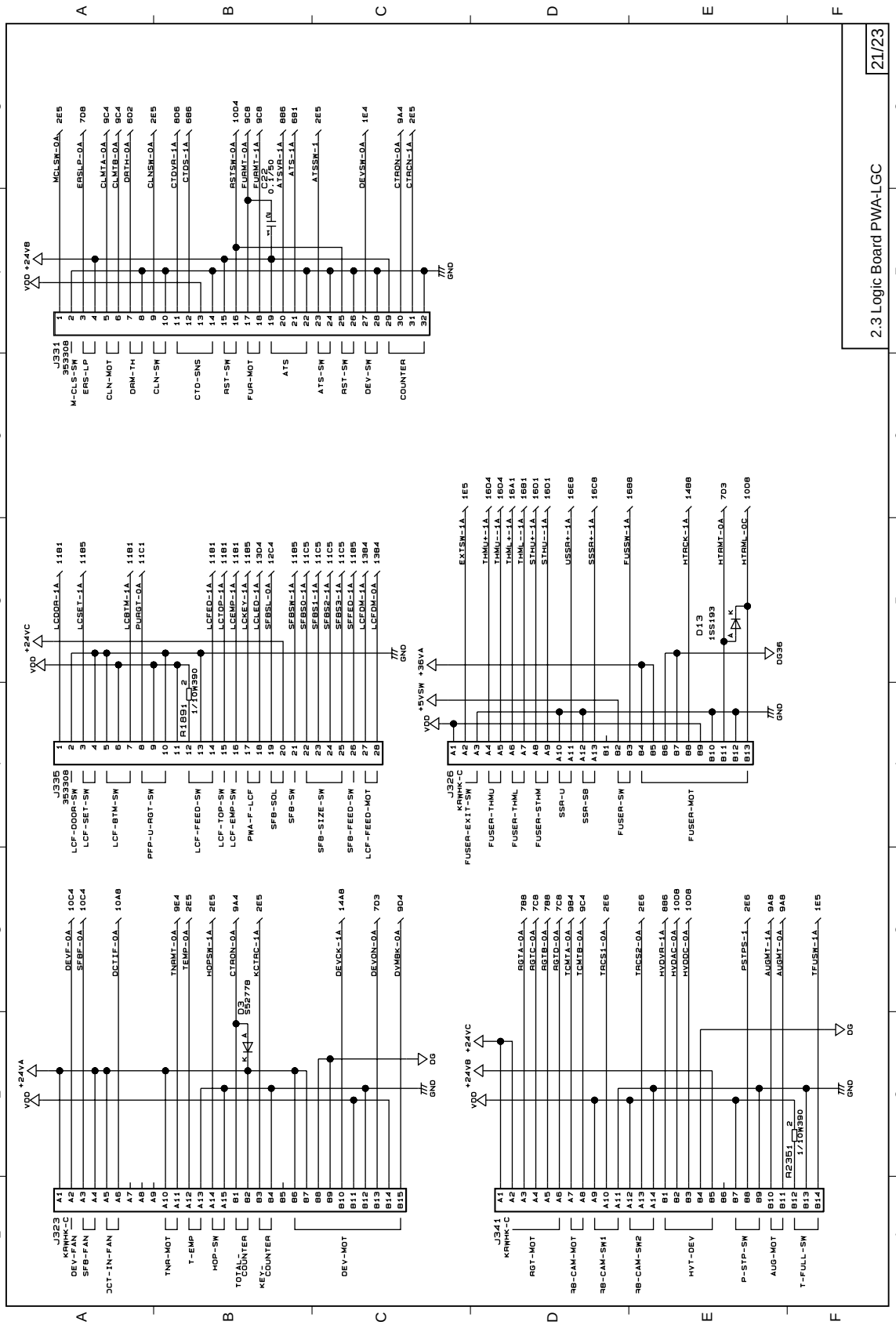

2.3 Logic Board PWA-LGC
16/23

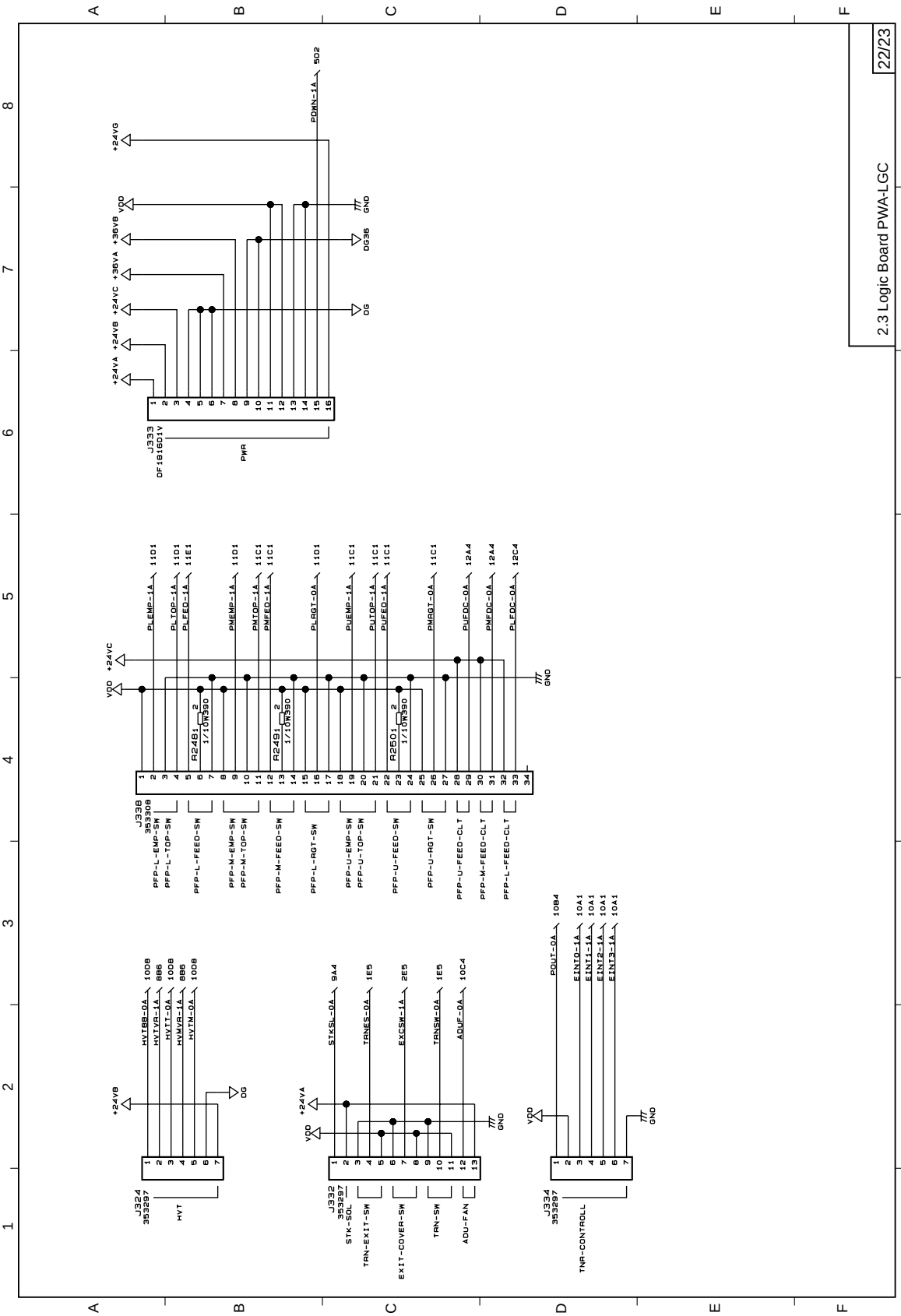

2.3 Logic Board PWA-LGC
17/23

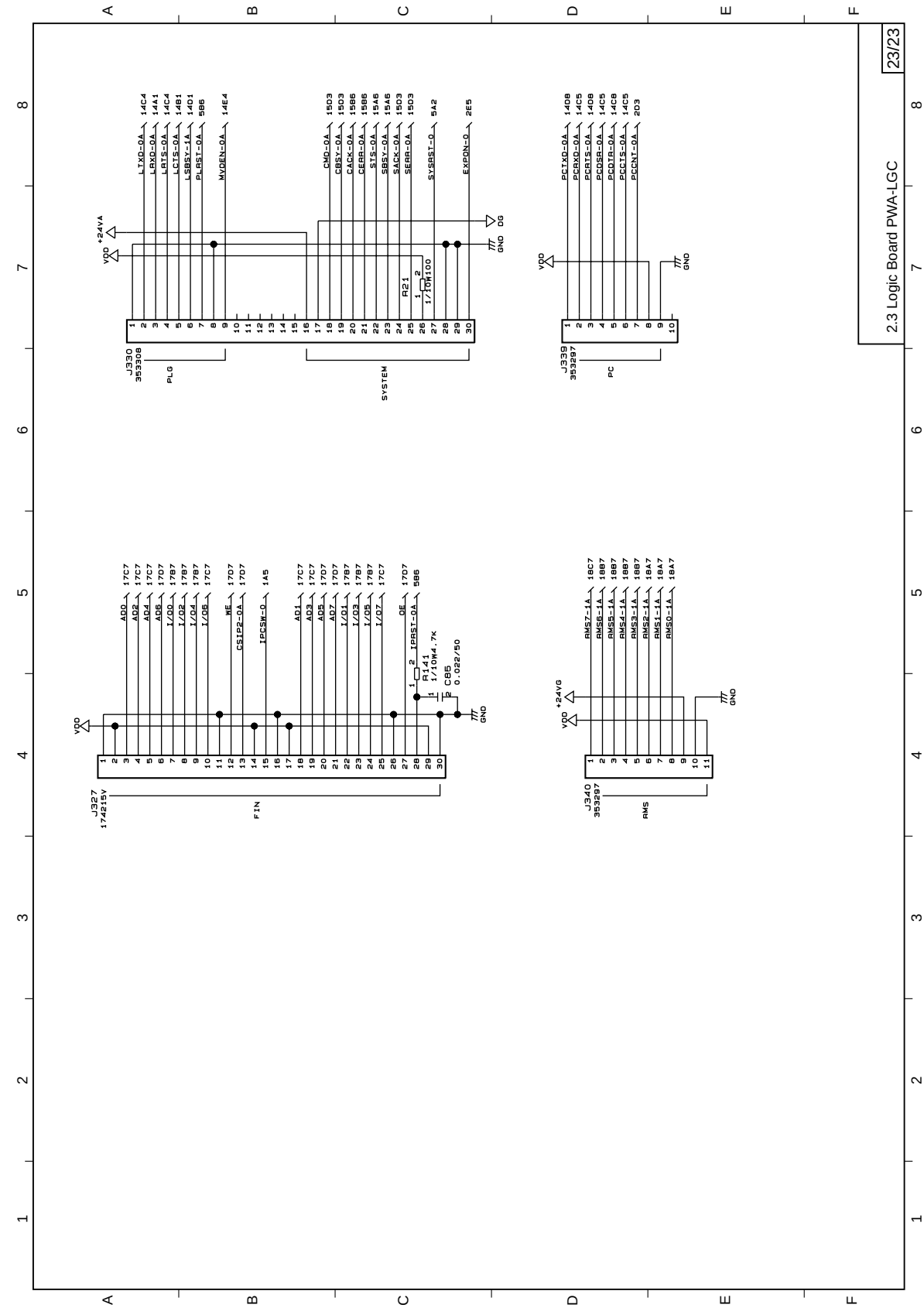

2.3 Logic Board PWA-LGC
18/23


2.3 Logic Board PWA-LGC
19/23

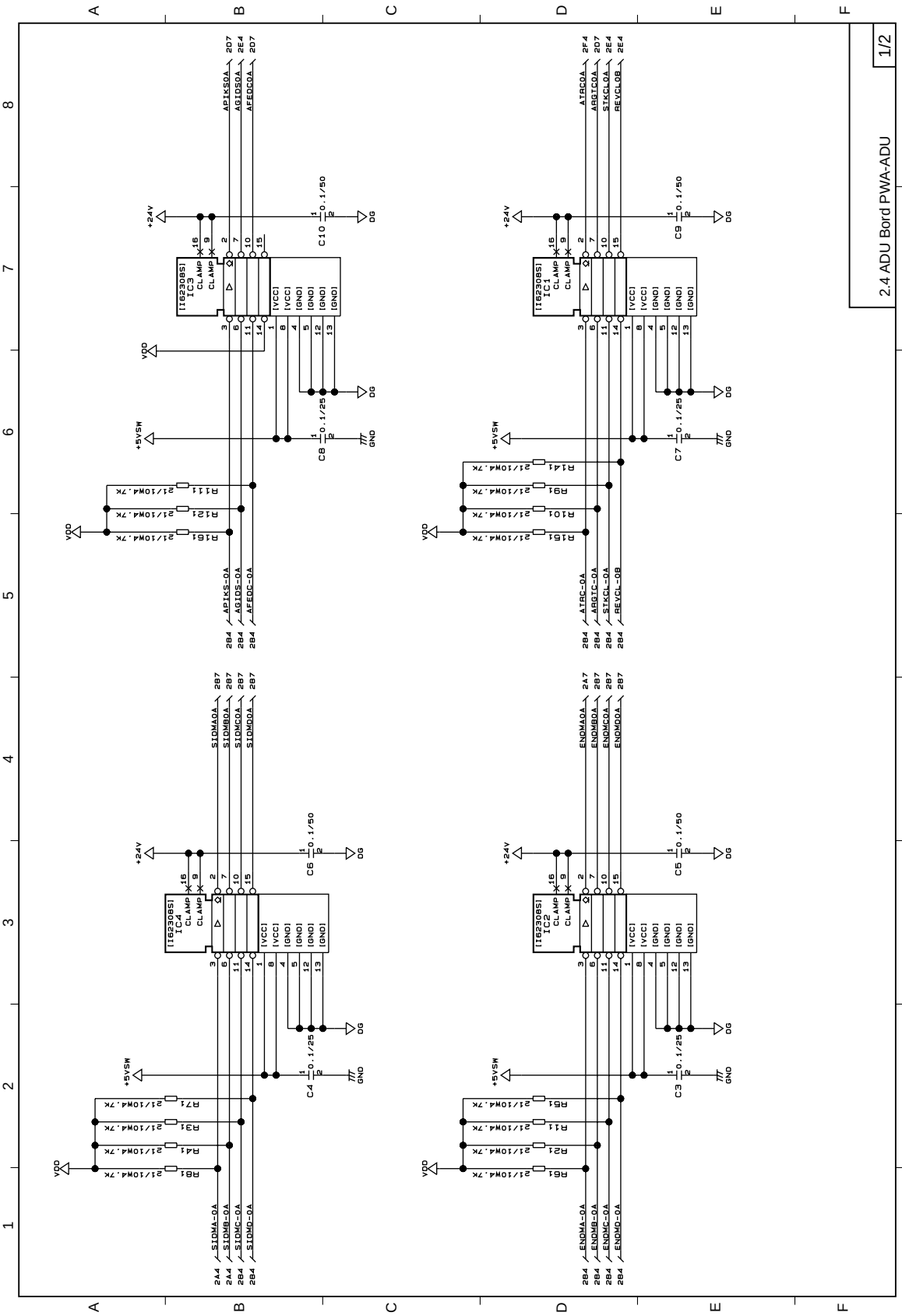

2.3 Logic Board PWA-LGC
20/23
J328
353308
PWA-F-ADU-300
J329
KRWHK-C
ADU-MOT
HTR-FAN
RVS-FAN
J325
KRWHK-C
PWA-F-MOT-300
SCRP-SOL
EXIT-FAN
DCT-OUT-FAN
HTR-FAN
J337
353297
PFP-CST-SW
J336
KRWHK-C
PFP-TRAY-MOT
PFP-RGT-CLT
PFP-MOT
LCF-TRAY-MOT

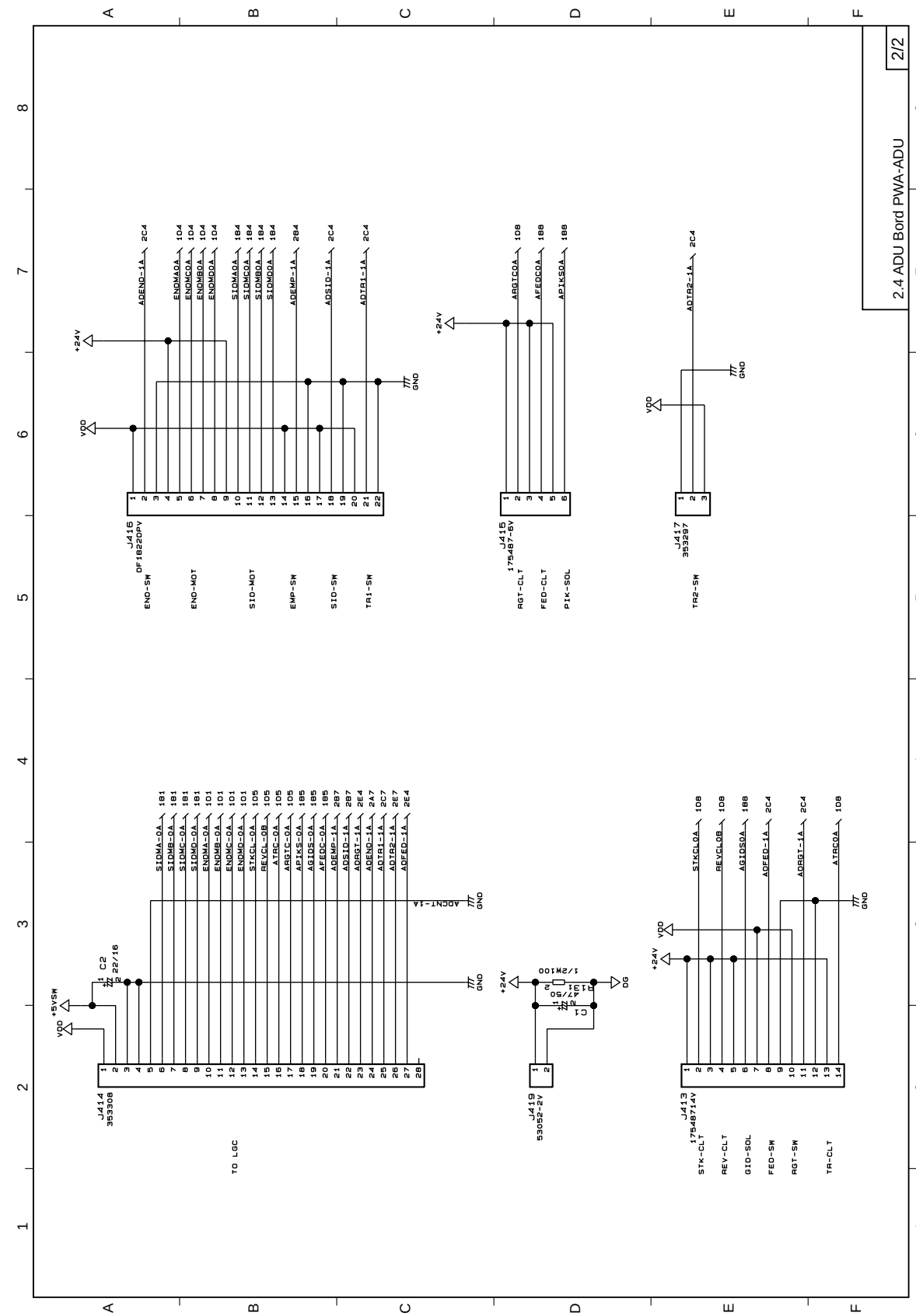

2.3 Logic Board PWA-LGC
21/23
J331
353308
M-CLS-SW
ERS-LP
CLN-MOT
DRM-TH
CLN-SW
CTO-SNS
RST-SW
FUR-MOT
ATS
ATS-SW
RST-SW
DEV-SW
COUNTER
VDD +24VB
GND
J335
353308
LCF-DOOR-SW
LCF-SET-SW
LCF-BTM-SW
PFP-U-RGT-SW
LCF-FEED-SW
LCF-TOP-SW
LCF-EMP-SW
PWA-F-LCF
SFB-SOL
SFB-SW
SFB-SIZE-SW
SFB-FEED-SW
LCF-FEED-MOT
VDD +24VC
R1891
1/10W390
J326
KRMHK-C
FUSER-EXIT-SW
FUSER-THMU
FUSER-THML
FUSER-STHM
SSR-U
SSR-SB
FUSER-SW
FUSER-MOT
VDD +5VSW
+36VA
D13
1SS193
D036
J323
KRMHK-C
DEV-FAN
SFB-FAN
JCT-IN-FAN
TNR-MOT
T-EMP
HOP-SW
TOTAL-COUNTER
KEY-COUNTER
DEV-MOT
VDD +24VA
D3
SS277B
GND
DG
J341
KRMHK-C
RGT-MOT
TB-CAM-MOT
TB-CAM-SW1
TB-CAM-SW2
HVT-DEV
P-STP-SW
AUG-MOT
T-FULL-SW
VDD +24VB
+24VC
R2351
1/10W390


2.3 Logic Board PWA-LGC
22/23
J333
DF1B16D1V
PWR
+24VA
+24VB
+24VC
+36VA
+36VB
VDD
+24VG
PDWN-1A 5D2
DG
DG36
GND
J338
353308
PFP-L-EMP-SW
PFP-L-TOP-SW
PFP-L-FEED-SW
PFP-M-EMP-SW
PFP-M-TOP-SW
PFP-M-FEED-SW
PFP-L-RGT-SW
PFP-U-EMP-SW
PFP-U-TOP-SW
PFP-U-FEED-SW
PFP-U-RGT-SW
PFP-U-FEED-CLT
PFP-M-FEED-CLT
PFP-L-FEED-CLT
PLEMP-1A 11D1
PLTOP-1A 11D1
PLFED-1A 11E1
PMEMP-1A 11D1
PMTOP-1A 11C1
PMFED-1A 11C1
PLRGT-0A 11D1
PUEMP-1A 11C1
PUTOP-1A 11C1
PUFED-1A 11C1
PMRGT-0A 11C1
PUFDC-0A 12A4
PMFDC-0A 12A4
PLFDC-0A 12C4
R2481 2 1/10W390
R2491 2 1/10W390
R2501 2 1/10W390
J324
353297
HVT
HVIBB-0A 10D8
HVIVR-1A 8B6
HVIT-0A 10D8
HVMVR-1A 8B6
HVTM-0A 10D8
J332
353297
STK-SOL
TRN-EXIT-SW
EXIT-COVER-SW
TRN-SW
ADU-FAN
STKSL-0A 9A4
TRNES-0A 1E5
EXCSW-1A 2E5
TRNSW-0A 1E5
ADUF-0A 10C4
J334
353297
TNR-CONTROLL
PDUT-0A 10B4
EINT0-1A 10A1
EINT1-1A 10A1
EINT2-1A 10A1
EINT3-1A 10A1

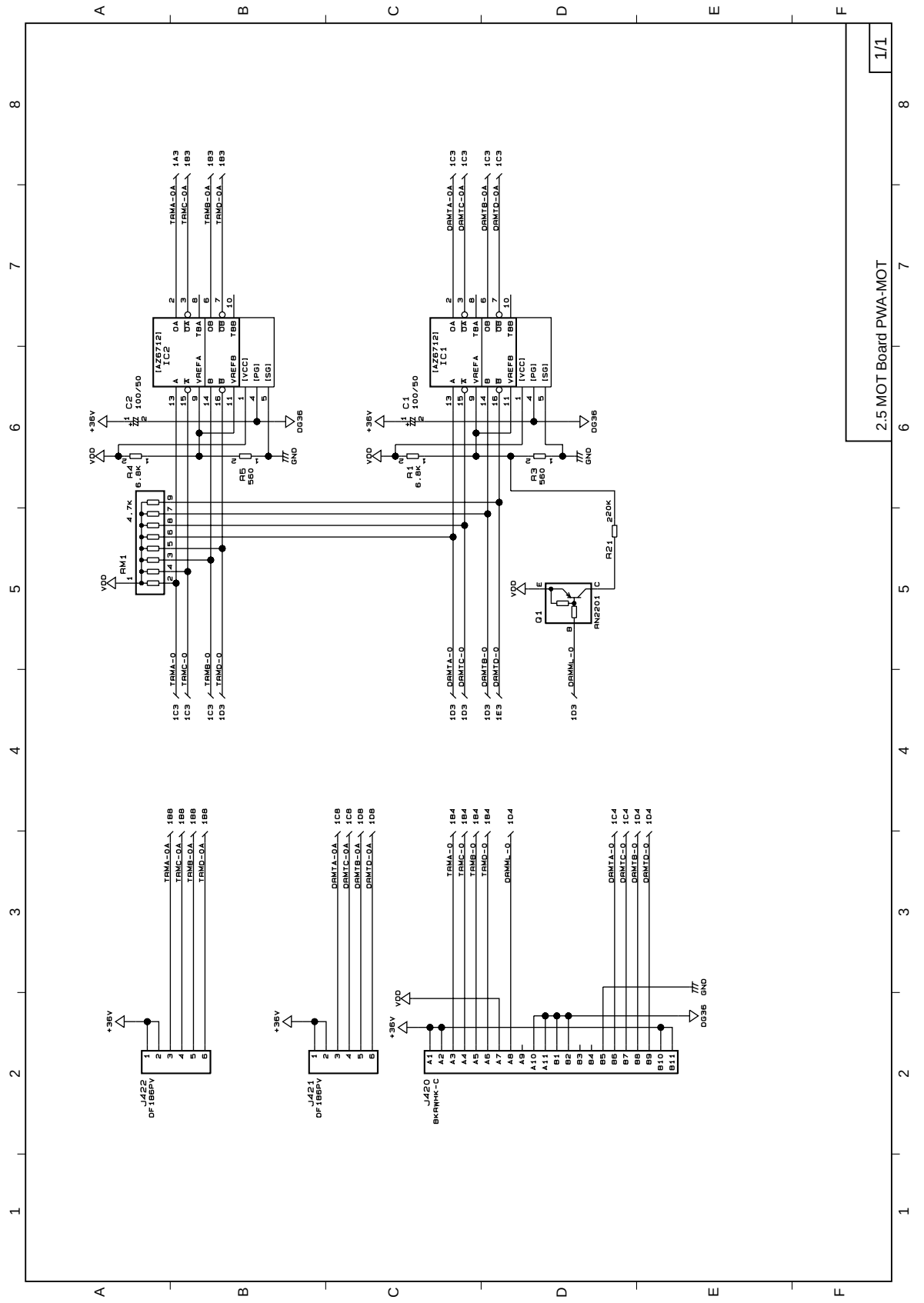

2.3 Logic Board PWA-LGC
23/23
J330
353308
PLG
SYSTEM
J339
353297
PC
J327
174215V
FIN
J340
353297
RMS
R21
1/10W100
R141
1/10W4.7K
C85
0.022/50
VDD
GND
+24VA
DG

2.4 ADU Board (PWA-ADU) 1/2~2/2

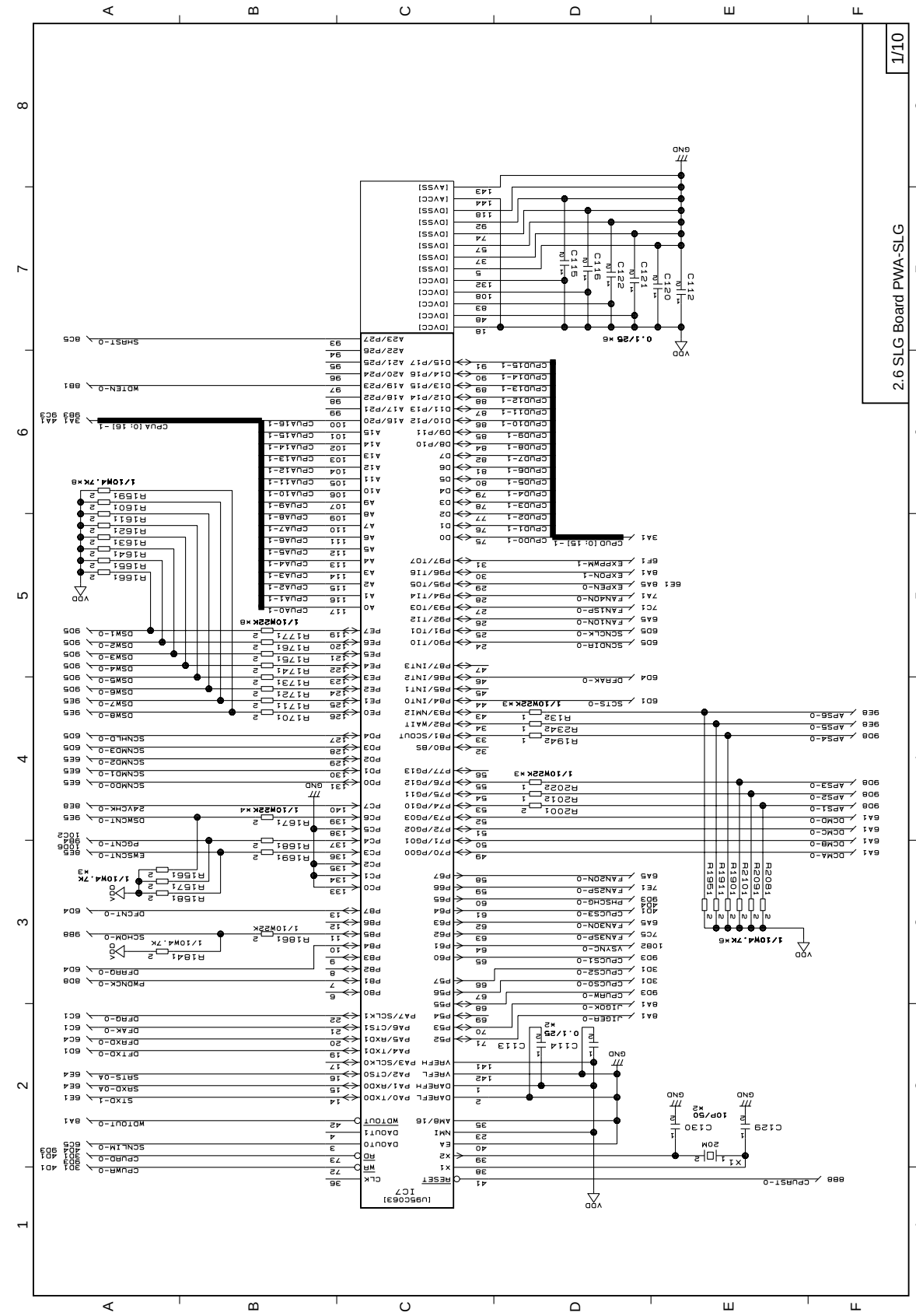


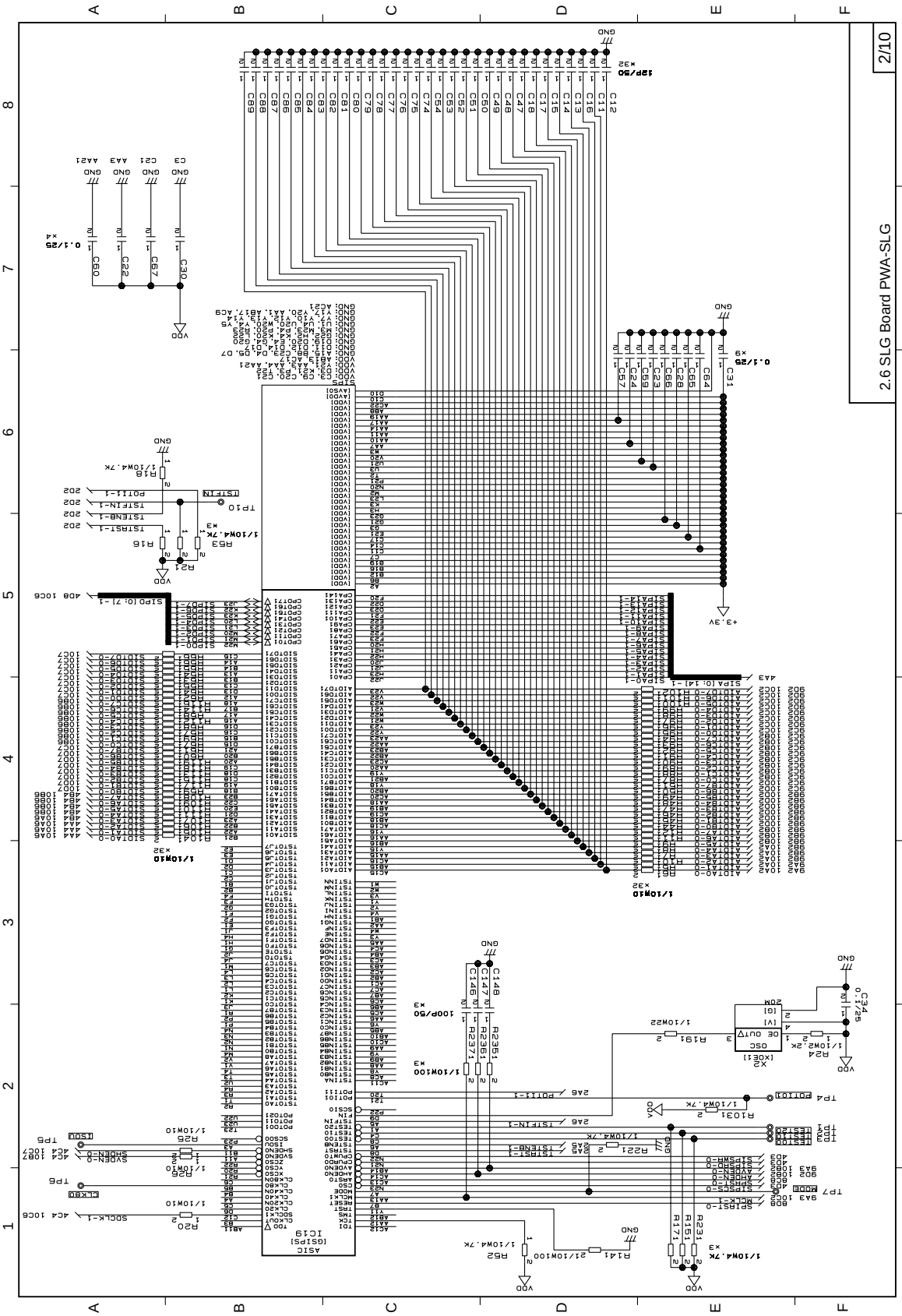

2.4 ADU Bord PWA-ADU
2/2
J416
DF1B22DPV
END-SW
END-MOT
SIO-MOT
EMP-SW
SIO-SW
TRI-SW
J415
175487-6V
RGT-CLT
FED-CLT
PIK-SOL
J417
353297
TR2-SW
J414
353308
TO LGC
J419
53052-2V
J413
175487714V
STK-CLT
REV-CLT
GID-SOL
FED-SW
RGT-SW
TR-CLT
+24V
VDD
GND
+5VSM
DG

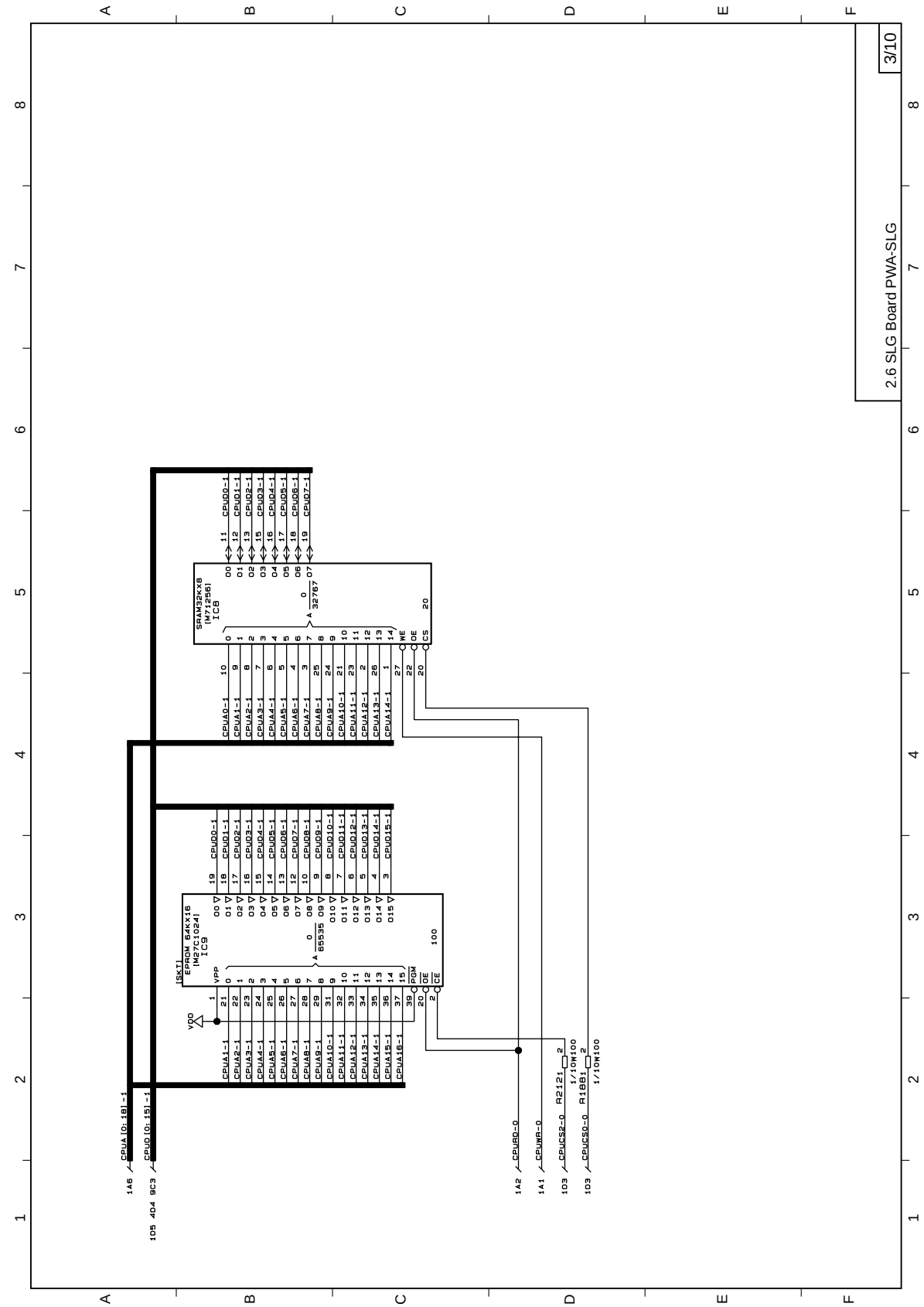
2.5 MOT Board (PWA-MOT) 1/1

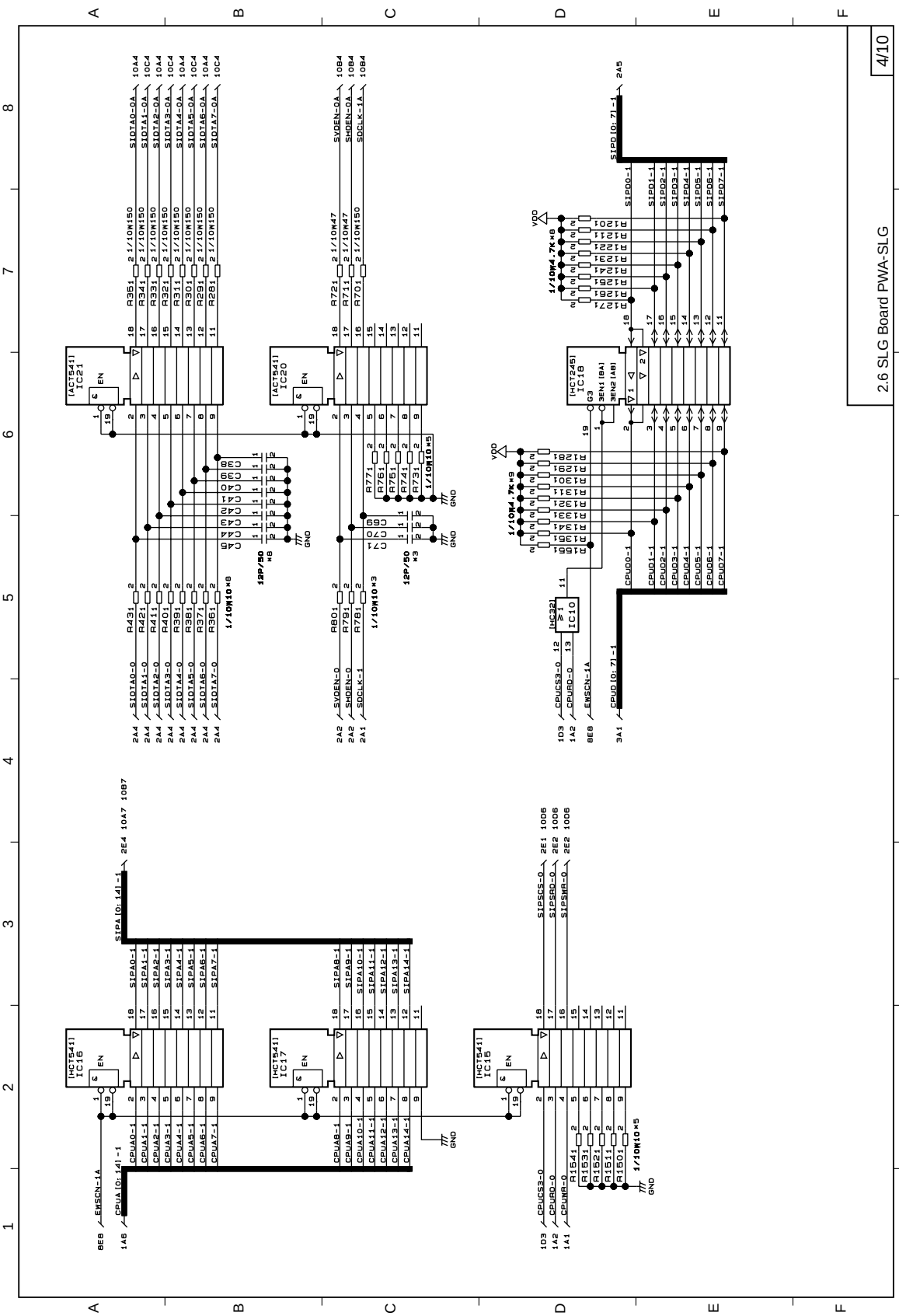


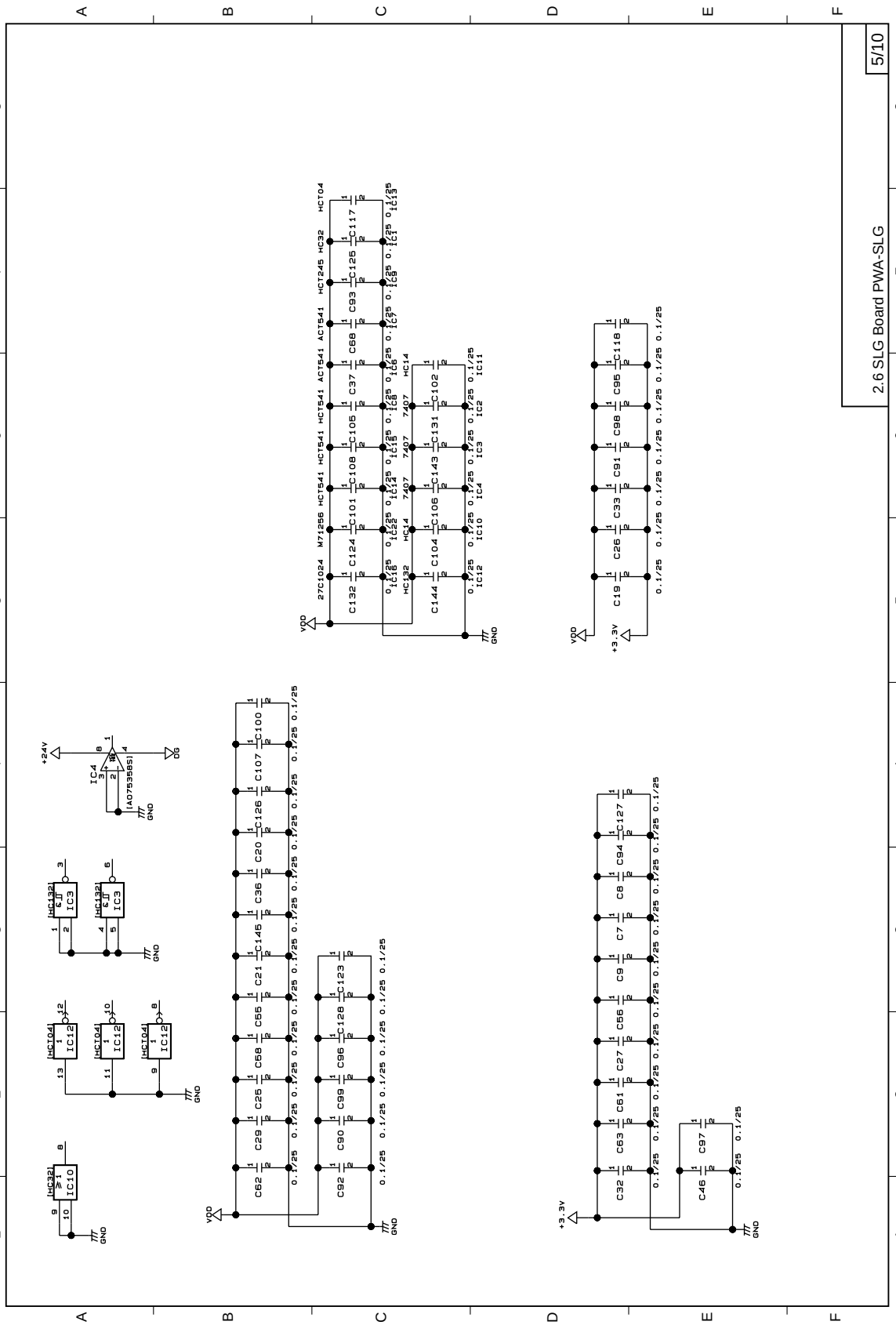
2.6 SLG Board (PWA-SLG) 1/10~10/10

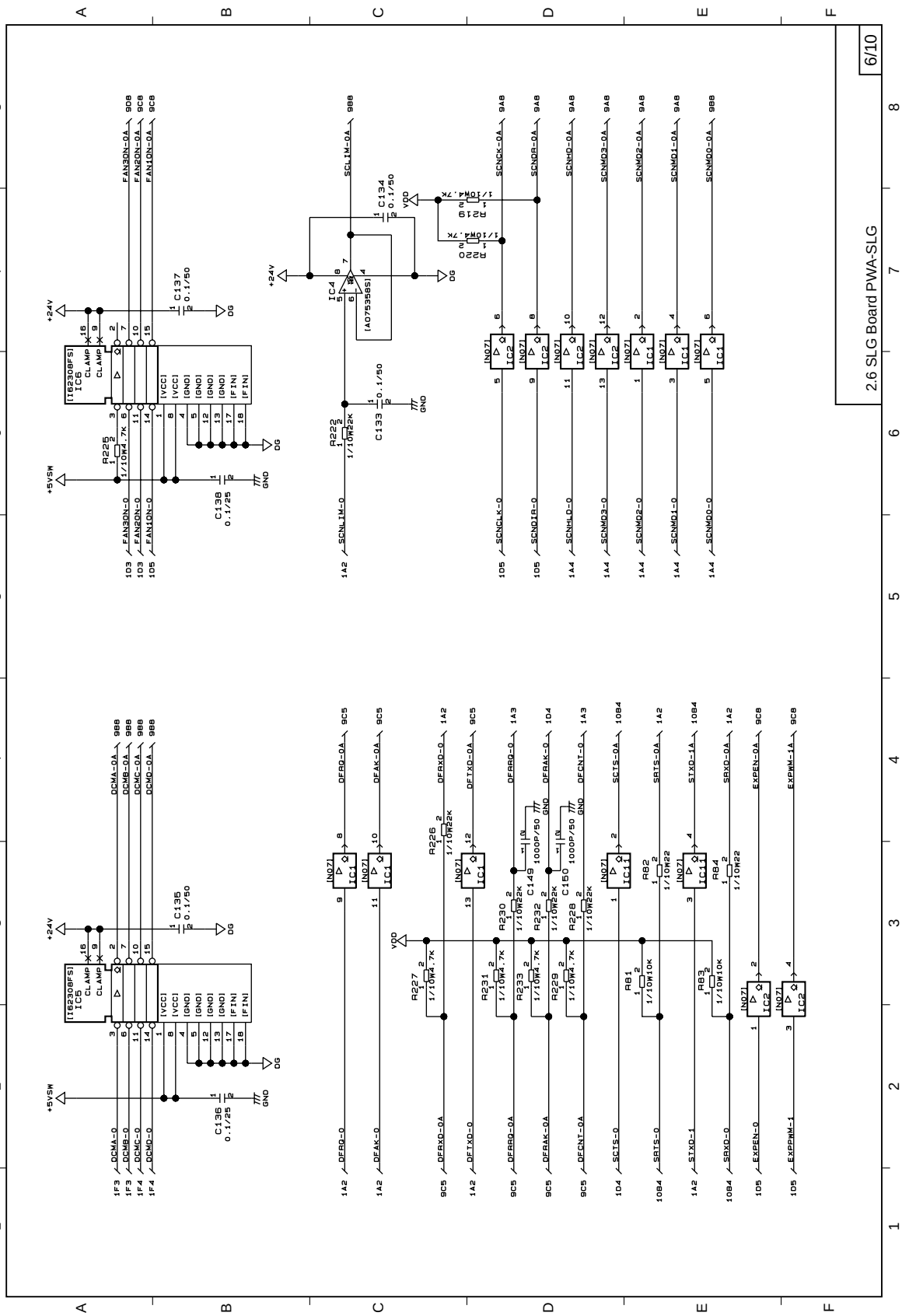


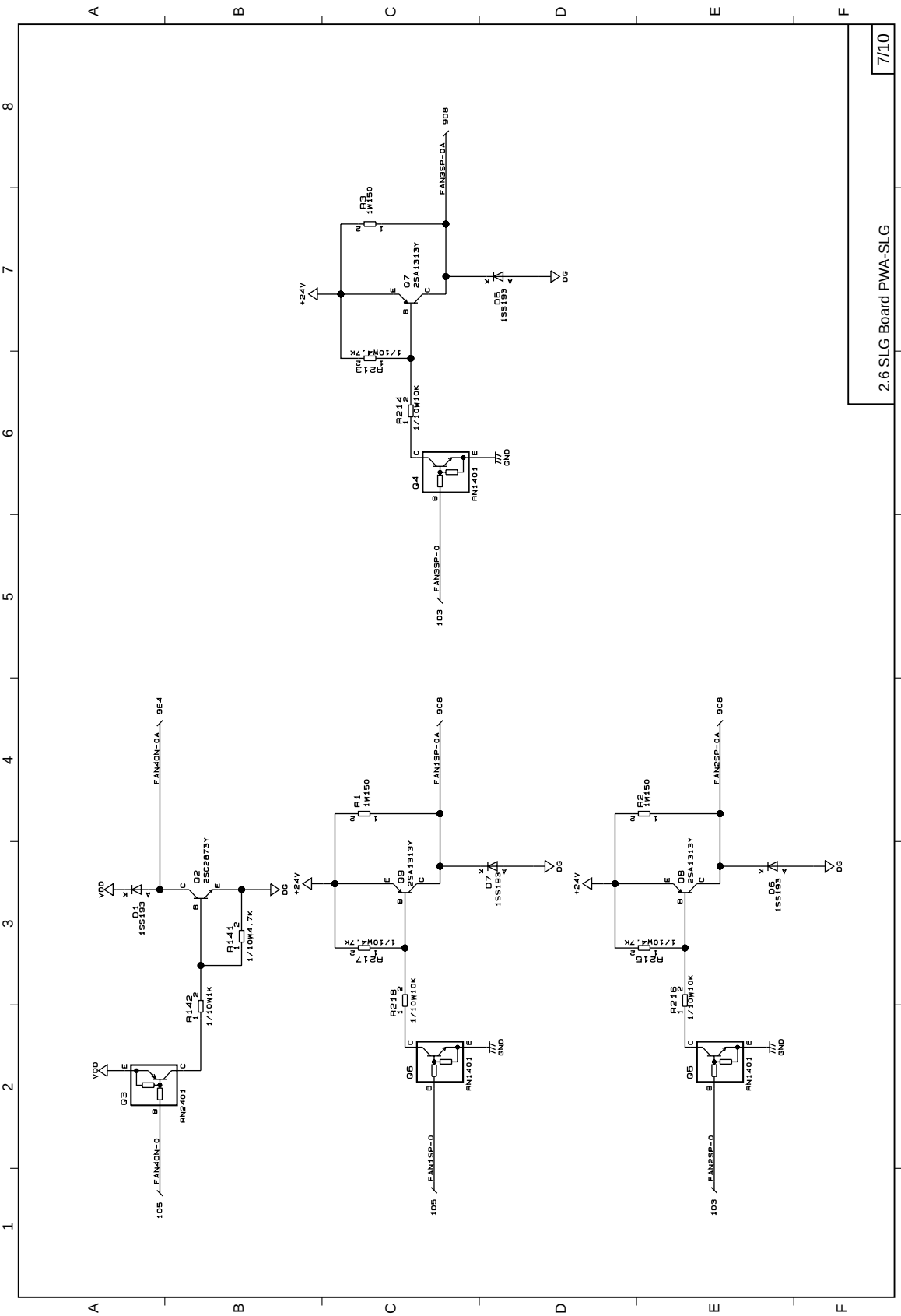

2/10
2.6 SLG Board PWA-SLG

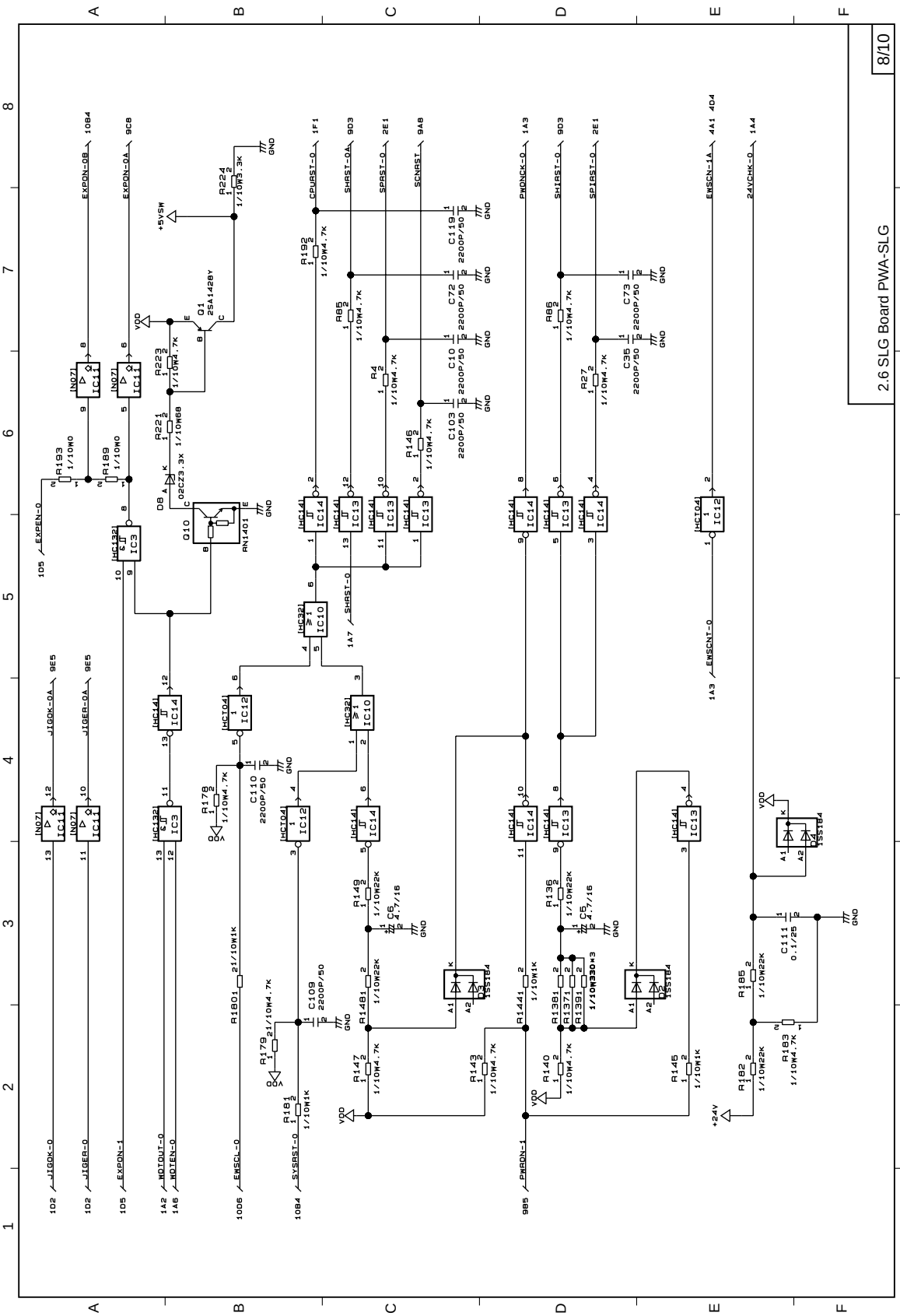

2.6 SLG Board PWA-SLG
3/10
SRAM32Kx8
(M71256)
IC8
EPROM 64Kx16
(M27C1024)
IC9
CPUA[0:18]-1
CPUD[0:15]-1
CPUA0-1
CPUA1-1
CPUA2-1
CPUA3-1
CPUA4-1
CPUA5-1
CPUA6-1
CPUA7-1
CPUA8-1
CPUA9-1
CPUA10-1
CPUA11-1
CPUA12-1
CPUA13-1
CPUA14-1
CPUA15-1
CPUA16-1
CPUD0-1
CPUD1-1
CPUD2-1
CPUD3-1
CPUD4-1
CPUD5-1
CPUD6-1
CPUD7-1
CPUD8-1
CPUD9-1
CPUD10-1
CPUD11-1
CPUD12-1
CPUD13-1
CPUD14-1
CPUD15-1
CPUR0-0
CPUWR-0
CPUCS2-0
CPUCS0-0
R2121
R1881
1/10W100
VDD
VPP
PGM
OE
CE
WE
CS

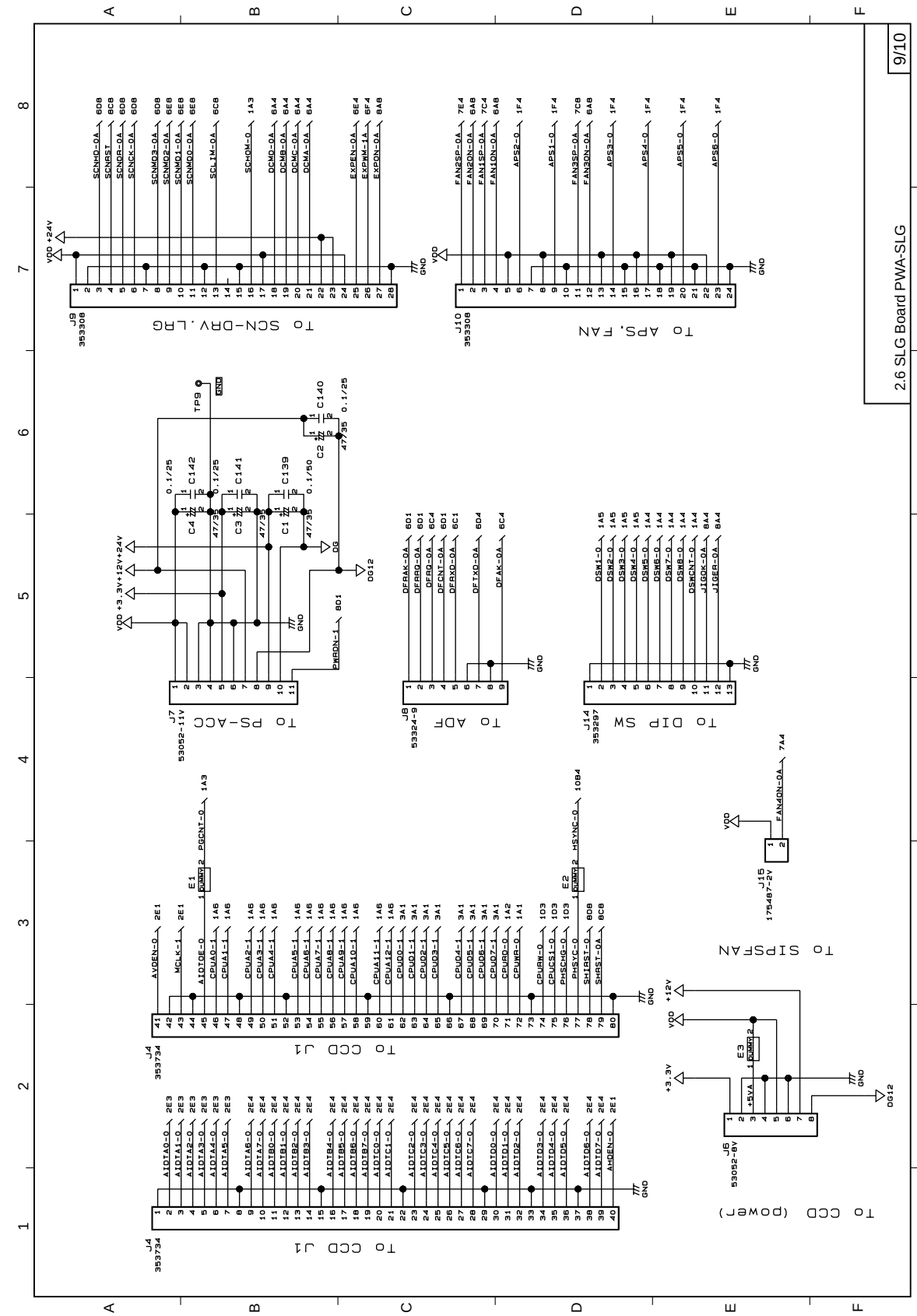

2.6 SLG Board PWA-SLG
4/10
[ACT541] IC21
[ACT541] IC20
[HCT541] IC16
[HCT541] IC17
[HCT541] IC15
[HCT245] IC18
[HC32] IC10
R431
R801
R351
R721
R1271
R1281
R1291
R1301
R1311
R1321
R1331
R1341
R1351
R1361
R1371
R1381
R1391
R1401
R1411
R1421
R1431
R1441
R1451
R1461
R1471
R1481
R1491
R1501
R1511
R1521
R1531
R1541
R771
R761
R751
R741
R731
R791
R781
R711
R701
R691
R681
R671
R661
R651
R641
R631
R621
R611
R601
R591
R581
R571
R561
R551
R541
R531
R521
R511
R501
R491
R481
R471
R461
R451
R441
R431
R421
R411
R401
R391
R381
R371
R361
R351
R341
R331
R321
R311
R301
R291
R281
C38
C39
C40
C41
C42
C43
C44
C45
C46
C47
C48
C49
C50
C51
C52
C53
C54
C55
C56
C57
C58
C59
C60
C61
C62
C63
C64
C65
C66
C67
C68
C69
C70
C71
1/10M10*8
1/10M10*3
1/10M10*5
12P/50 *8
12P/50 *3
1/10M4.7K*8
1/10M4.7K*9
1/10M150
1/10M47
GND
VDD
SIPA[0:14]-1
CPUA[0:14]-1
CPUD[0:7]-1
SIPD[0:7]-1
SIOTA0-0
SIOTA1-0
SIOTA2-0
SIOTA3-0
SIOTA4-0
SIOTA5-0
SIOTA6-0
SIOTA7-0
SVOEN-0
SHOEN-0
SDCLK-1A
EWSCN-1A
CPUCS3-0
CPUWR-0
CPURD-0
SIPSCS-0
SIPSWR-0
SIPSWE-0
CPUD0-1
CPUD1-1
CPUD2-1
CPUD3-1
CPUD4-1
CPUD5-1
CPUD6-1
CPUD7-1
SIPD0-1
SIPD1-1
SIPD2-1
SIPD3-1
SIPD4-1
SIPD5-1
SIPD6-1
SIPD7-1
SIPA0-1
SIPA1-1
SIPA2-1
SIPA3-1
SIPA4-1
SIPA5-1
SIPA6-1
SIPA7-1
SIPA8-1
SIPA9-1
SIPA10-1
SIPA11-1
SIPA12-1
SIPA13-1
SIPA14-1
CPUA0-1
CPUA1-1
CPUA2-1
CPUA3-1
CPUA4-1
CPUA5-1
CPUA6-1
CPUA7-1
CPUA8-1
CPUA9-1
CPUA10-1
CPUA11-1
CPUA12-1
CPUA13-1
CPUA14-1
3EN1(BA)
3EN2(AB)
G3
G

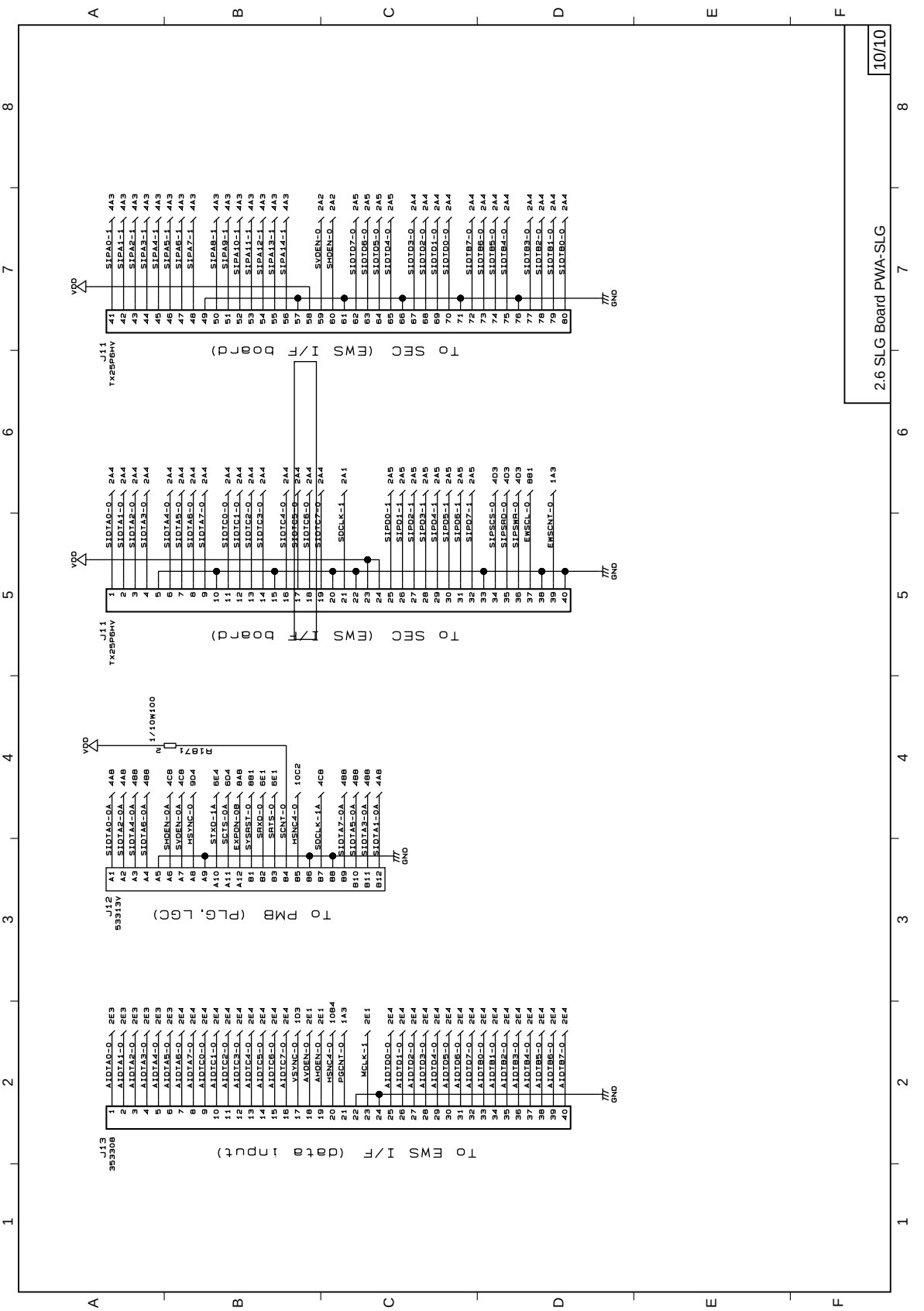

2.6 SLG Board PWA-SLG
5/10


2.6 SLG Board PWA-SLG
6/10

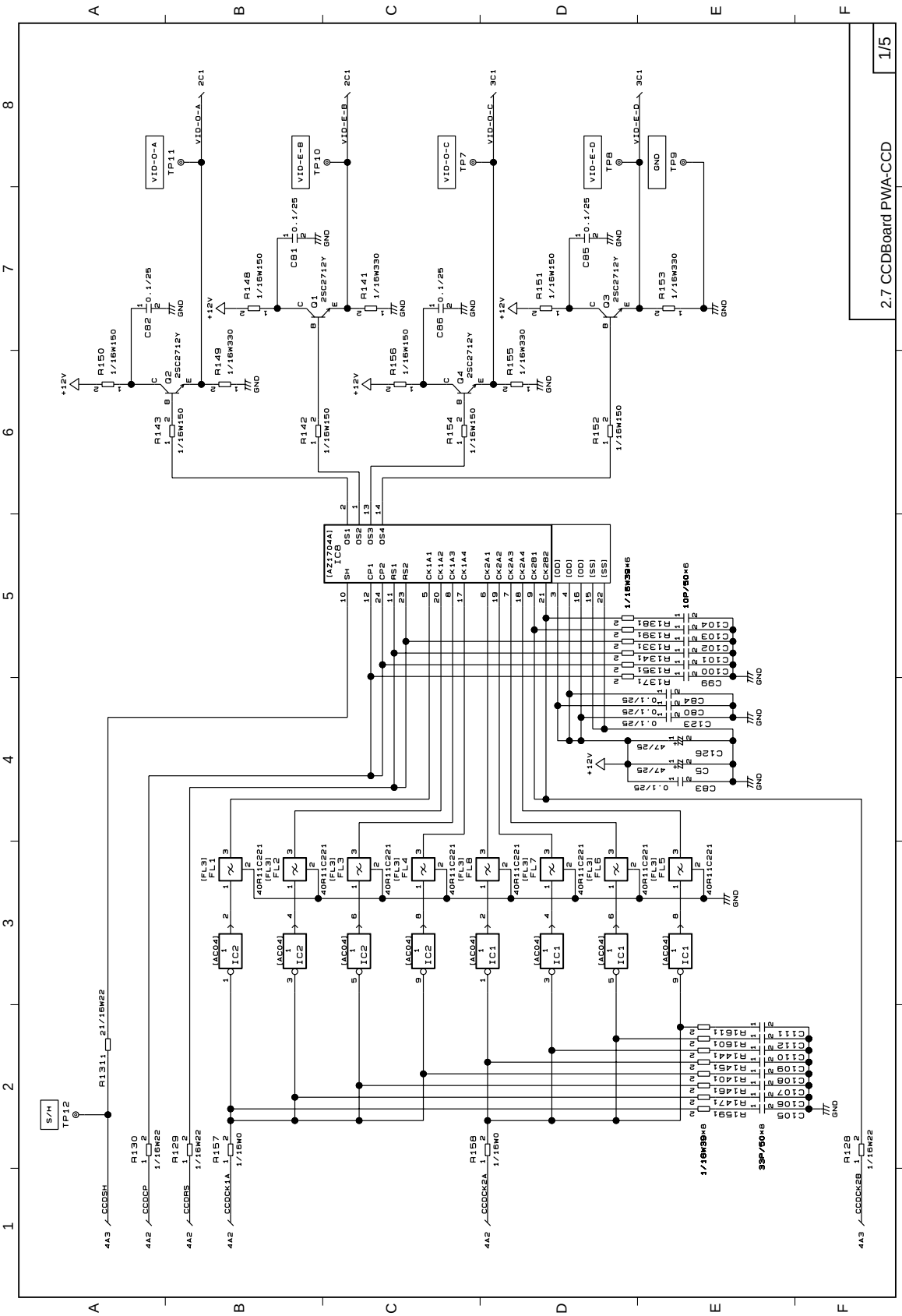

2.6 SLG Board PWA-SLG
7/10
FAN40N-0A
FAN1SP-0A
FAN2SP-0A
FAN3SP-0A
+24V
VDD
DG
GND
Q1 1SS193
Q2 2SC2873Y
Q3 RN2401
Q4 RN1401
Q5 RN1401
Q6 RN1401
Q7 2SA1313Y
Q8 2SA1313Y
Q9 2SA1313Y
D5 1SS193
D6 1SS193
D7 1SS193
R1 1W150
R2 1W150
R3 1W150
R141 1/10W4.7K
R142 1/10W1K
R214 1/10W10K
R215 1/10W10K
R216 1/10W10K
R217 1/10W4.7K
R218 1/10W10K
R219 1/10W4.7K
105 FAN40N-0
105 FAN1SP-0
103 FAN2SP-0
103 FAN3SP-0
9E4
9C8
9C8
9D8

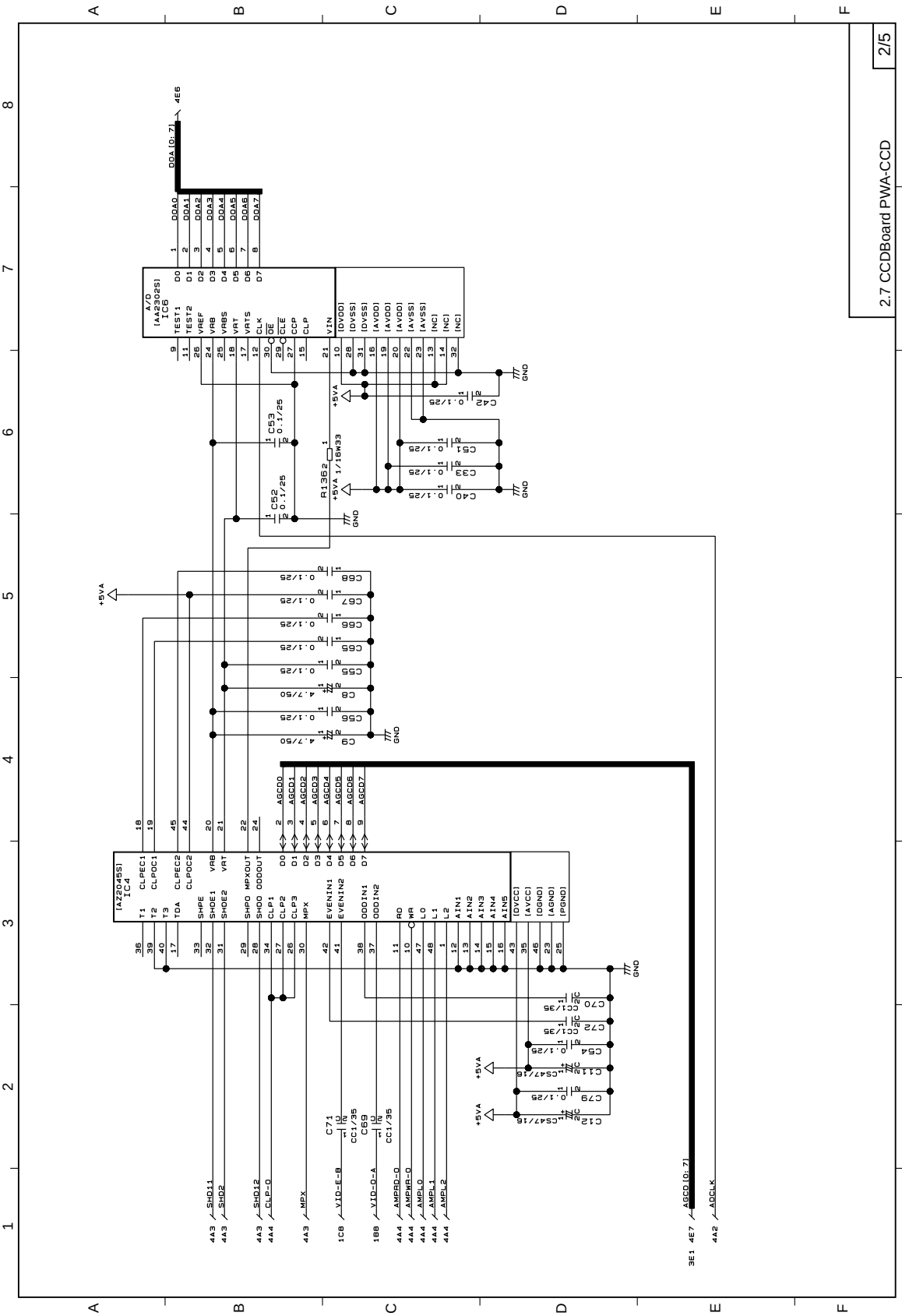

2.6 SLG Board PWA-SLG
8/10

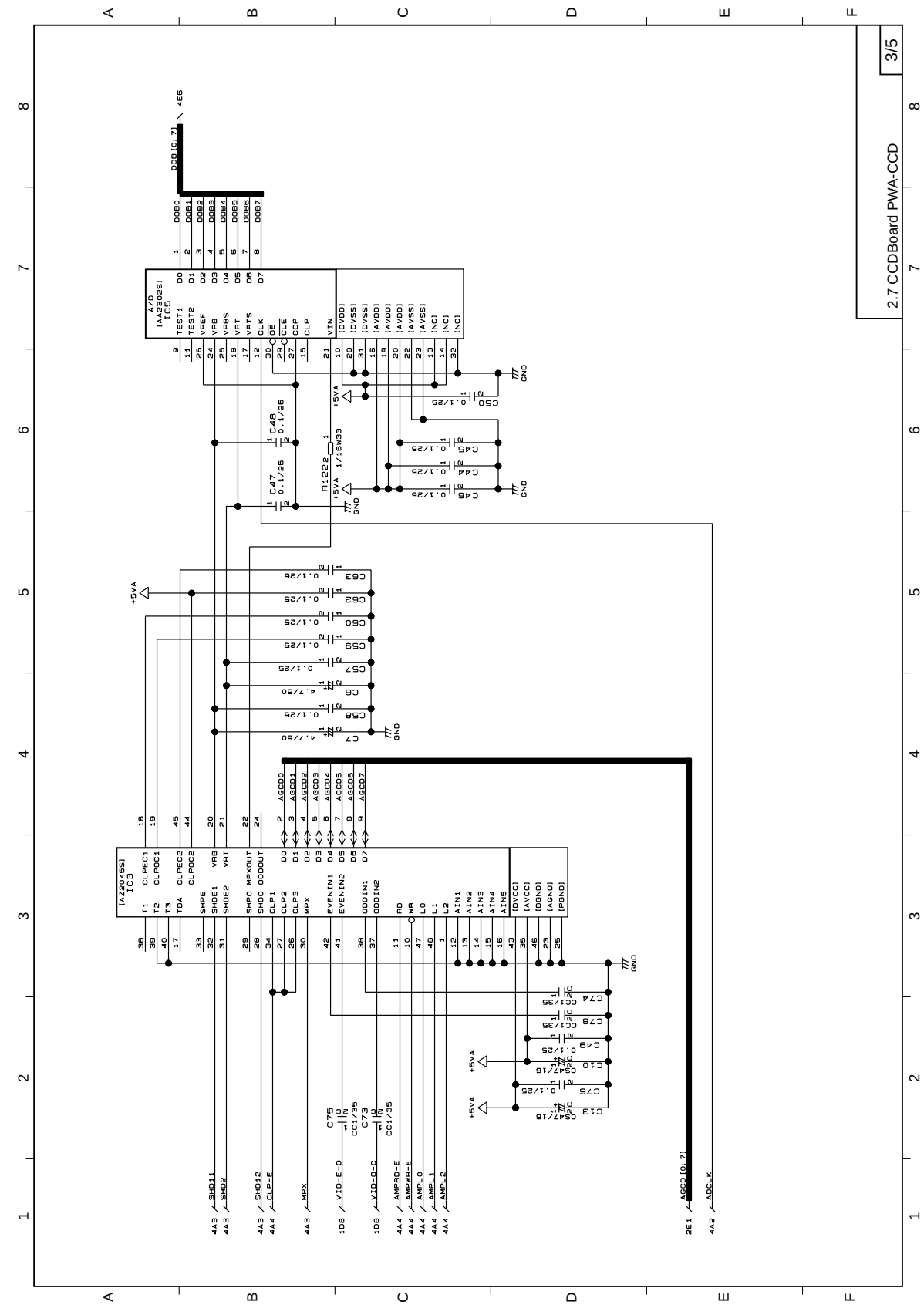

2.6 SLG Board PWA-SLG
9/10
To SCN-DRV.LRG
To APS, FAN
To PS-ACC
To ADF
To DIP SW
To CCD J1
To CCD J1
To CCD (power)
To SIPSFAN

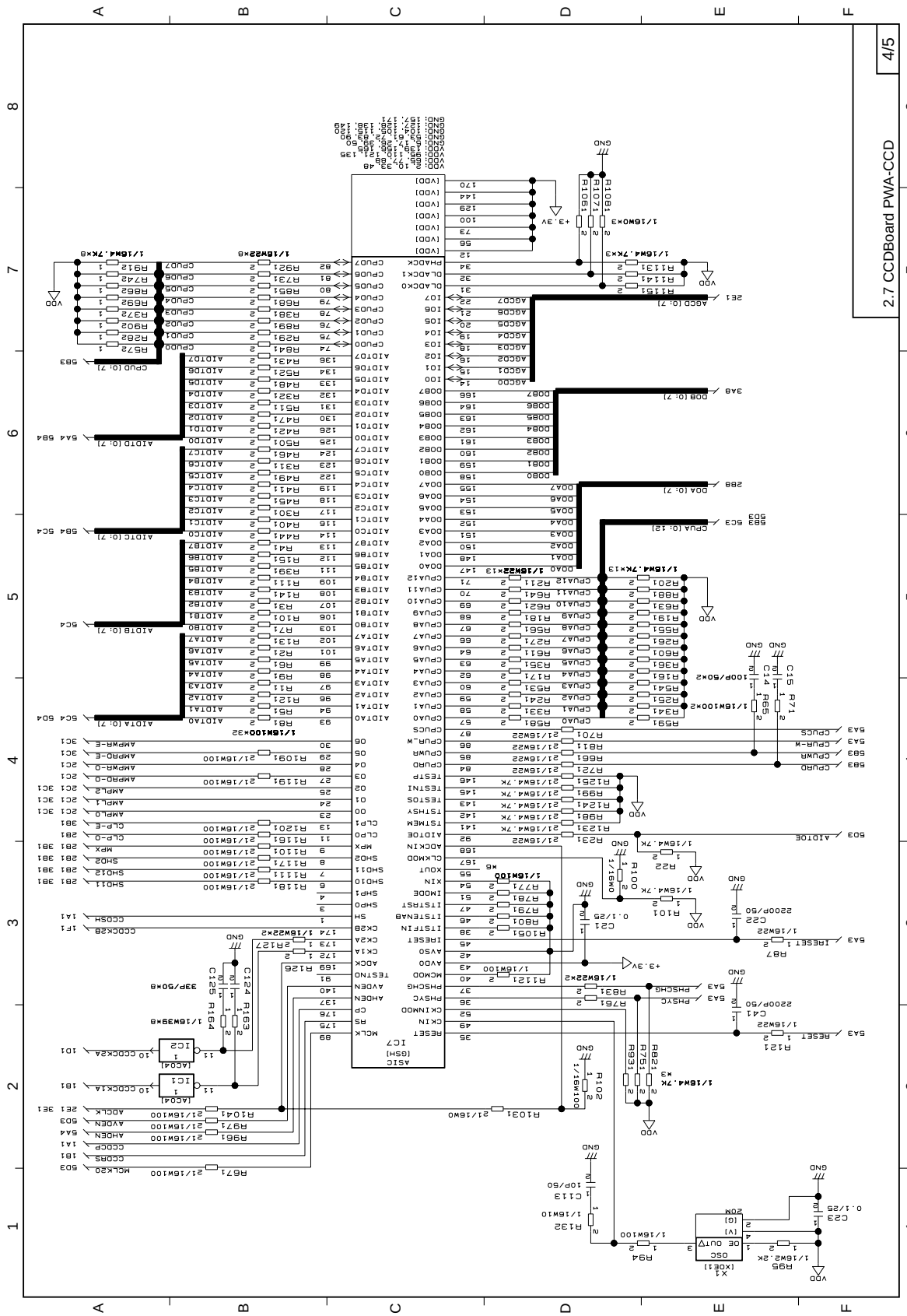

2.6 SLG Board PWA-SLG
10/10
To EWS I/F (data input)
To PMB (PLG, LGC)
To SEC (EWS I/F board)
To SEC (EWS I/F board)

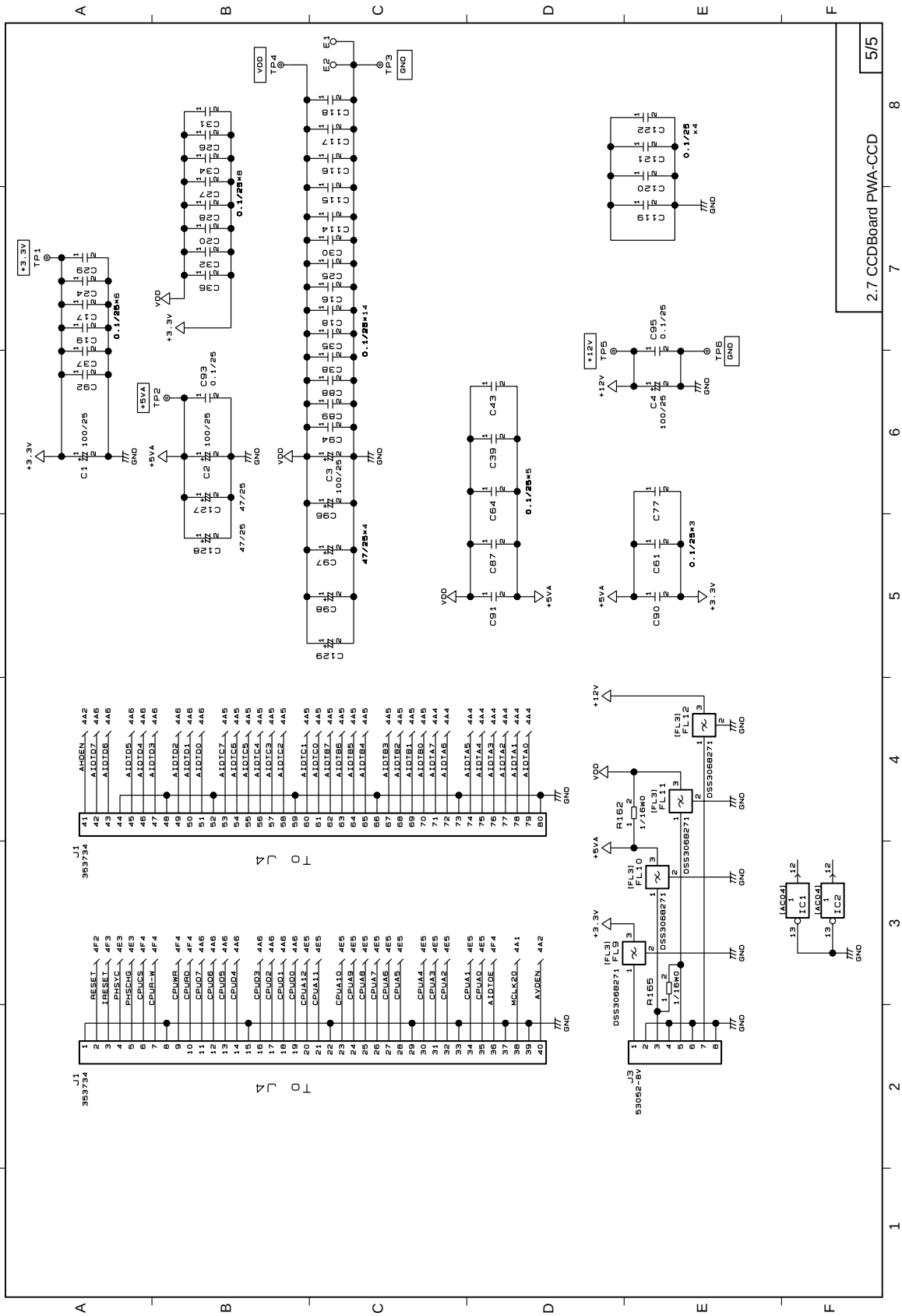
2.7 CCD Board (PWA-CCD) 1/5~5/5



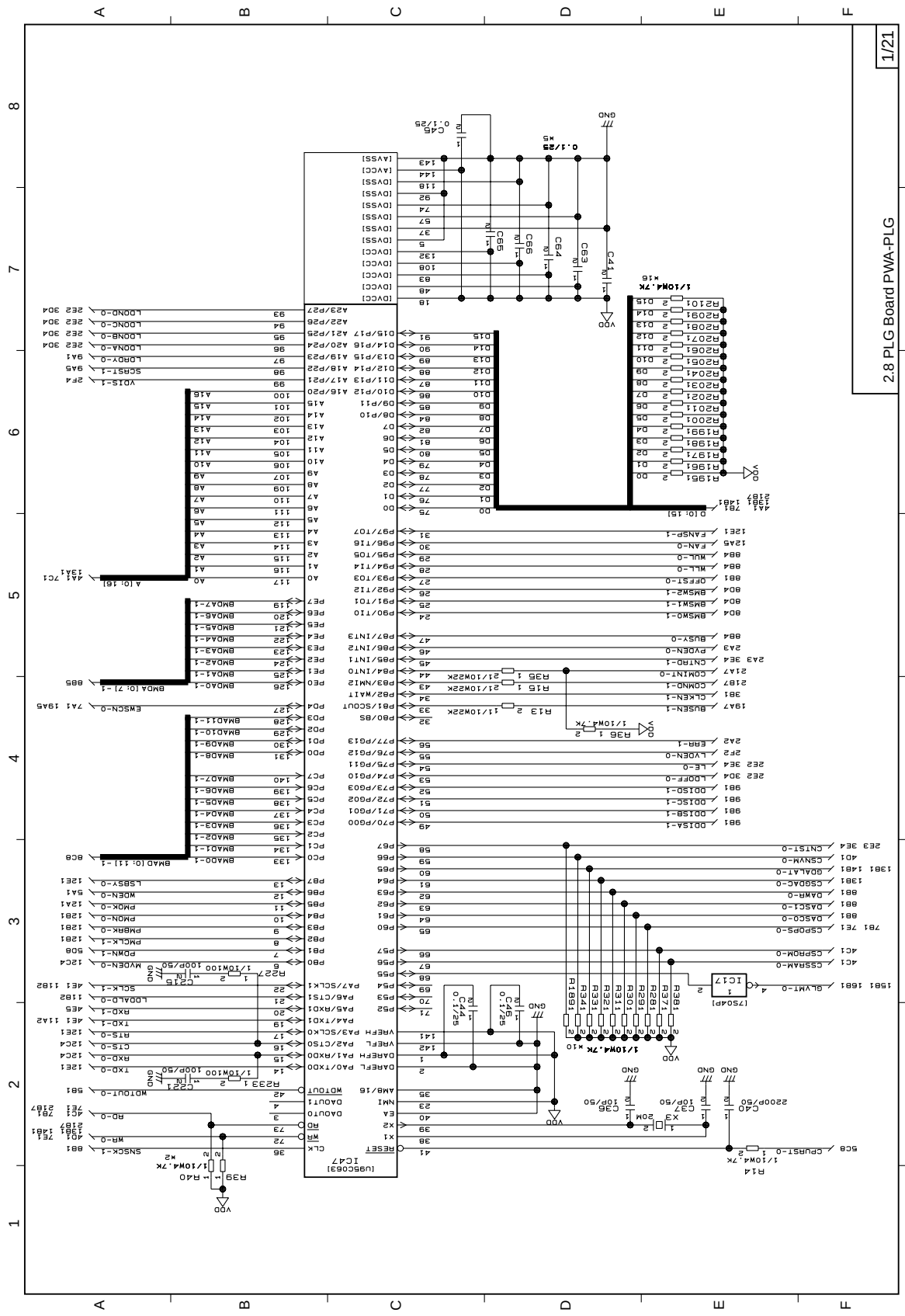

2.7 CCDBoard PWA-CCD
2/5
A/D (AA2302S) IC5
(AZ2045S) IC4
R1362
+5VA
GND
AGCD[0:7]
ADCLK
SHD11
SHD12
SHD2
CLP-O
MPX
VID-E-B
VID-O-A
AMPRD-O
AMPWR-O
AMPL-O
AMPL-1
AMPL-2

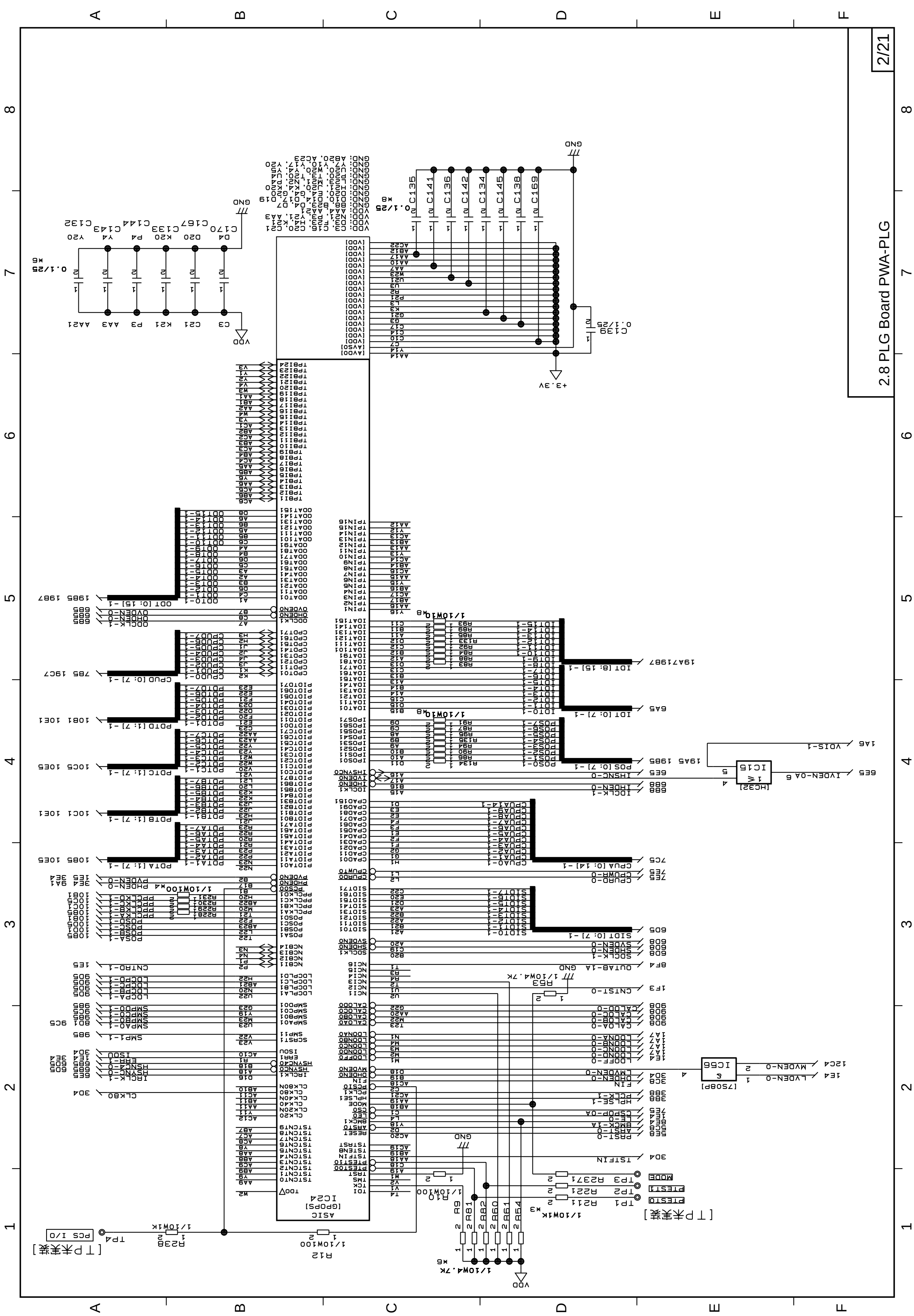

2.7 CCDBoard PWA-CCD
3/5

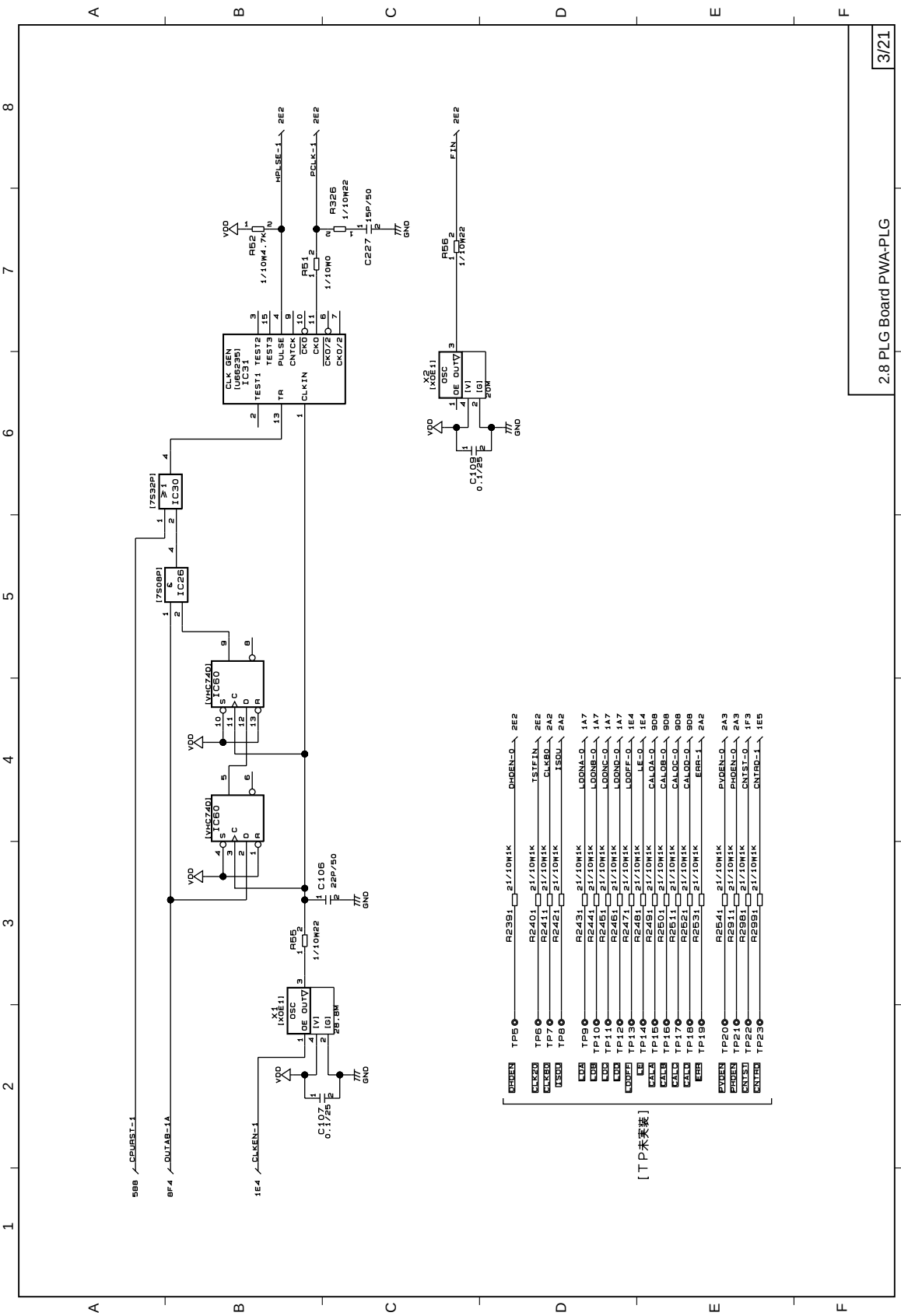

4/5
2.7 CCDBoard PWA-CCD

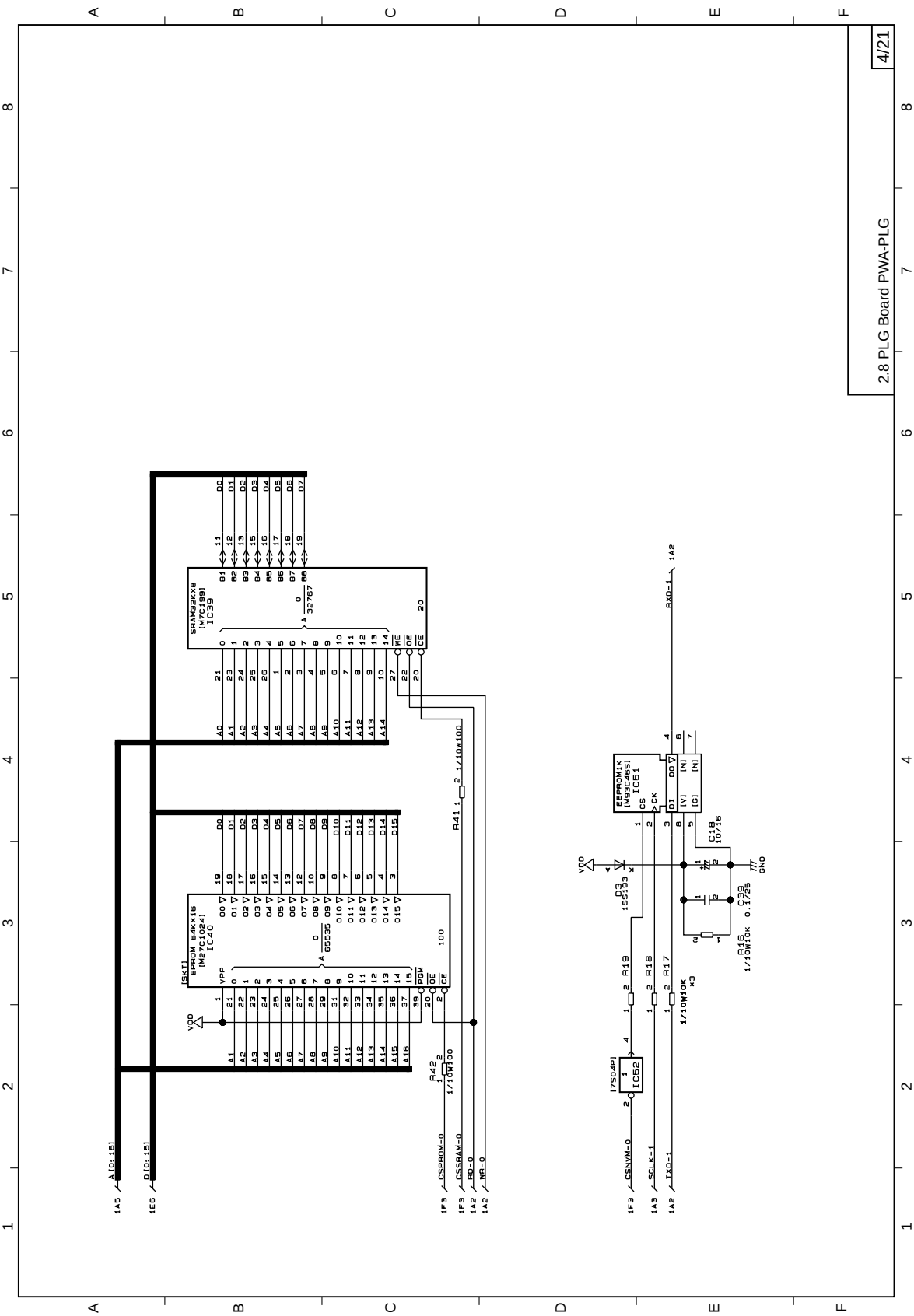

2.7 CCDBoard PWA-CCD
5/5

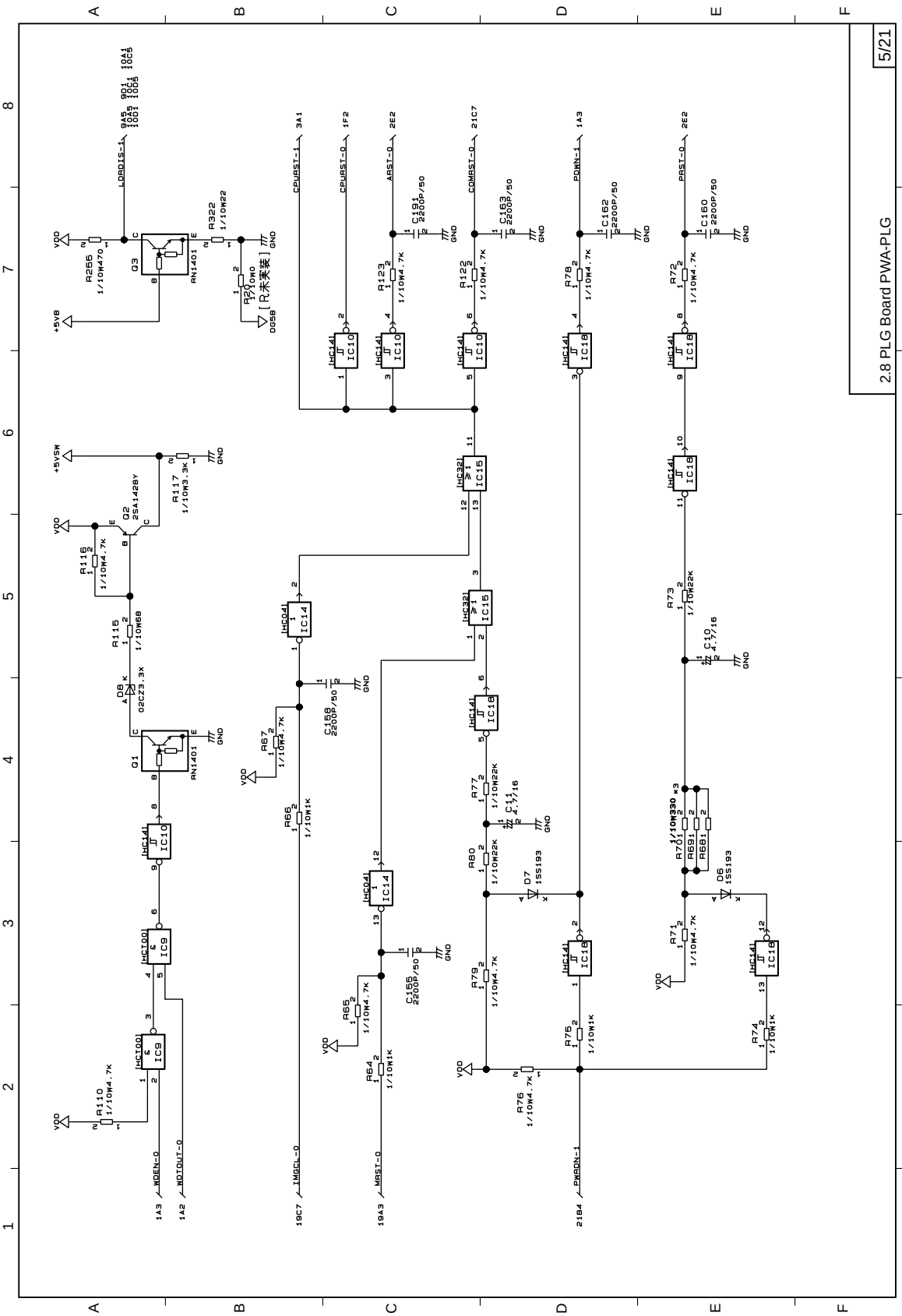
2.8 PLG Board (PWA-PLG) 1/21~21/21

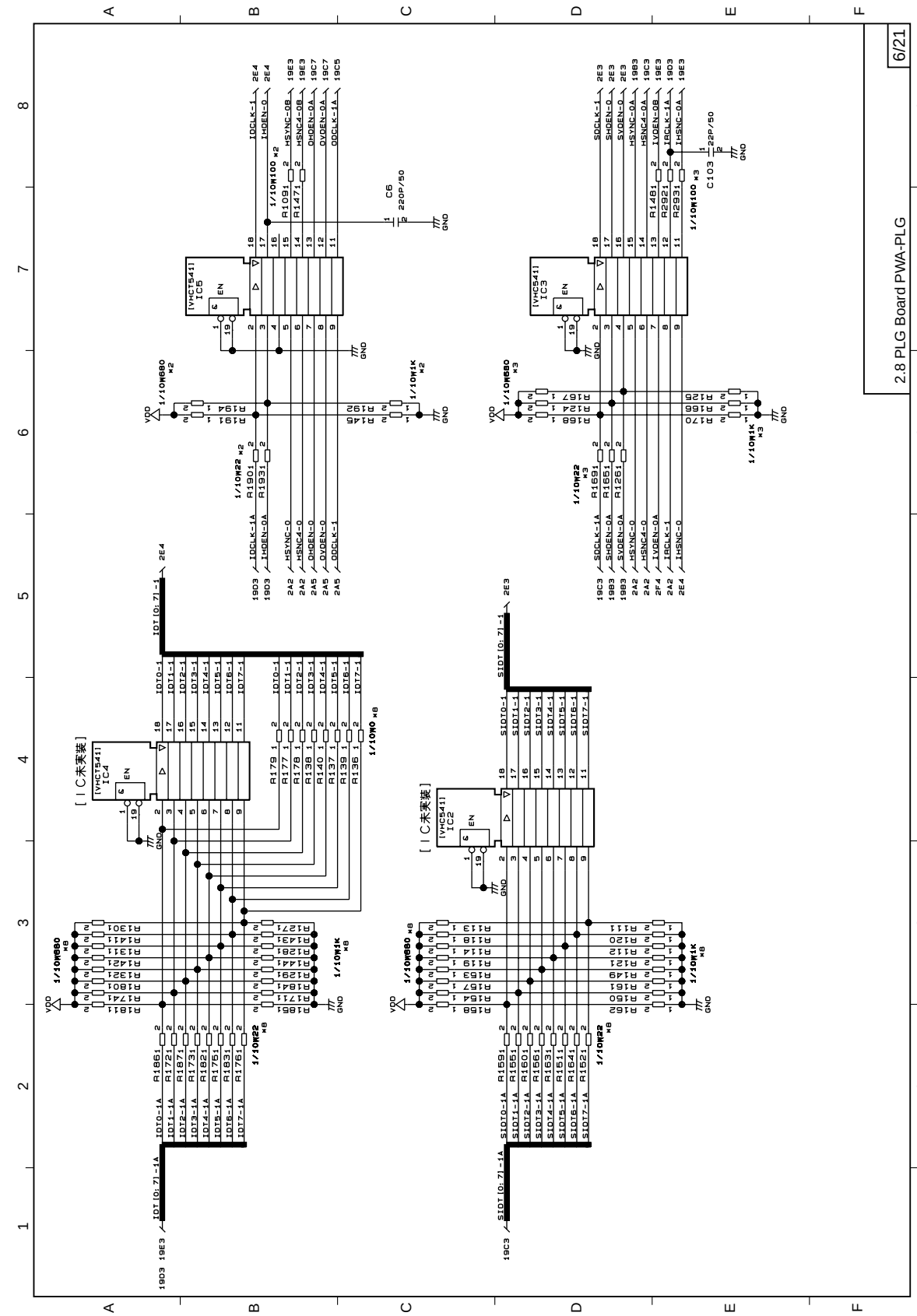


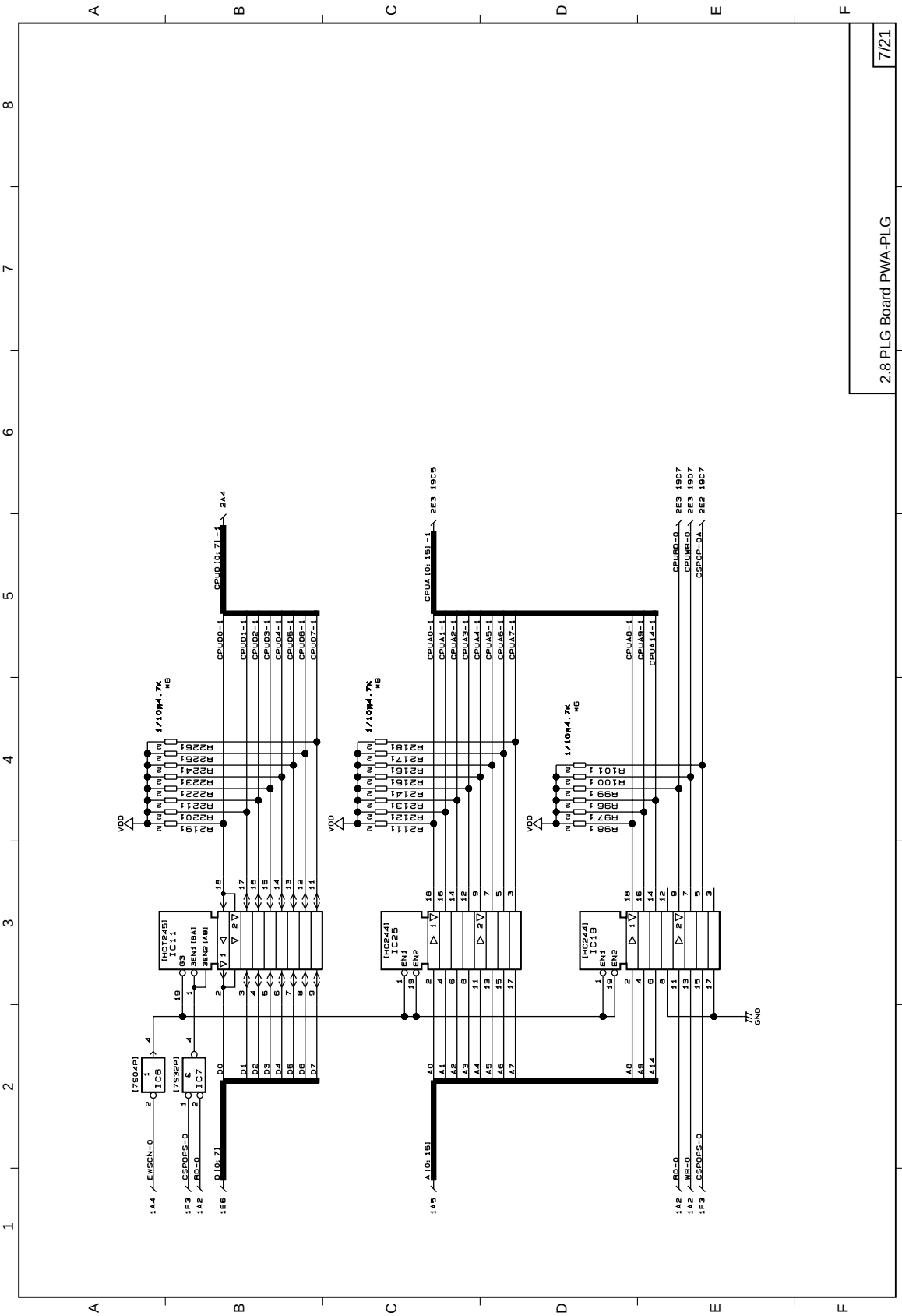

2.8 PLG Board PWA-PLG
2/21

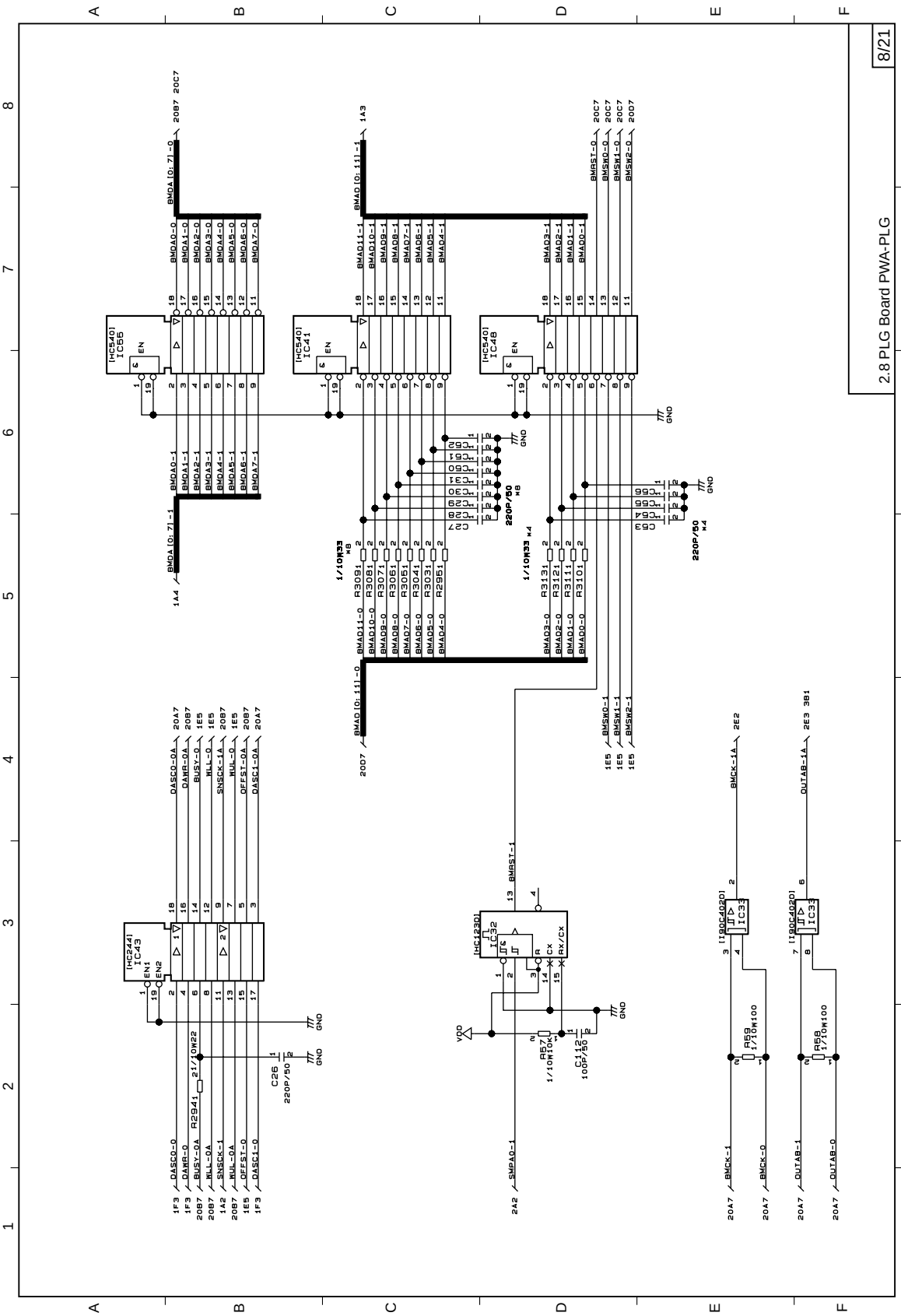

2.8 PLG Board PWA-PLG
3/21
CLK GEN
[U6625S]
IC31
CLKIN
TEST1
TEST2
TEST3
PULSE
CNTCK
CKO
CKO/8
CKO/2
TA
HPLSE-1
PCLK-1
FIN
R52
R51
R326
R66
C227
C106
C107
C108
X1
X2
OSC
OE
OUTY
[TSC32P]
IC30
[7S08P]
IC26
[VHC74D]
IC60
VDD
GND
CPURST-1
OUTAB-1A
CLKEN-1
[TP未実装]
DHDEN
CLKA0
CLKB0
TSDU
TP5
TP6
TP7
TP8
R2391
R2401
R2411
R2421
DHDEN-0
TSFIN
CLKB0
TSDU
CDA
CDB
CDC
CDD
LDOFF
LE
CALA
CALB
CALC
CALD
ERR
TP90
TP100
TP110
TP120
TP130
TP140
TP150
TP160
TP170
TP180
TP190
R2431
R2441
R2451
R2461
R2471
R2481
R2491
R2501
R2511
R2521
R2531
LDDNA-0
LDDNB-0
LDDNC-0
LDDND-0
LDOFF-0
LE-0
CALOA-0
CALOB-0
CALOC-0
CALOD-0
ERR-1
PVDEN
PHDEN
CNTST
CNTRD
TP200
TP210
TP220
TP230
R2541
R2911
R2881
R2991
PVDEN-0
PHDEN-0
CNTST-0
CNTRD-1

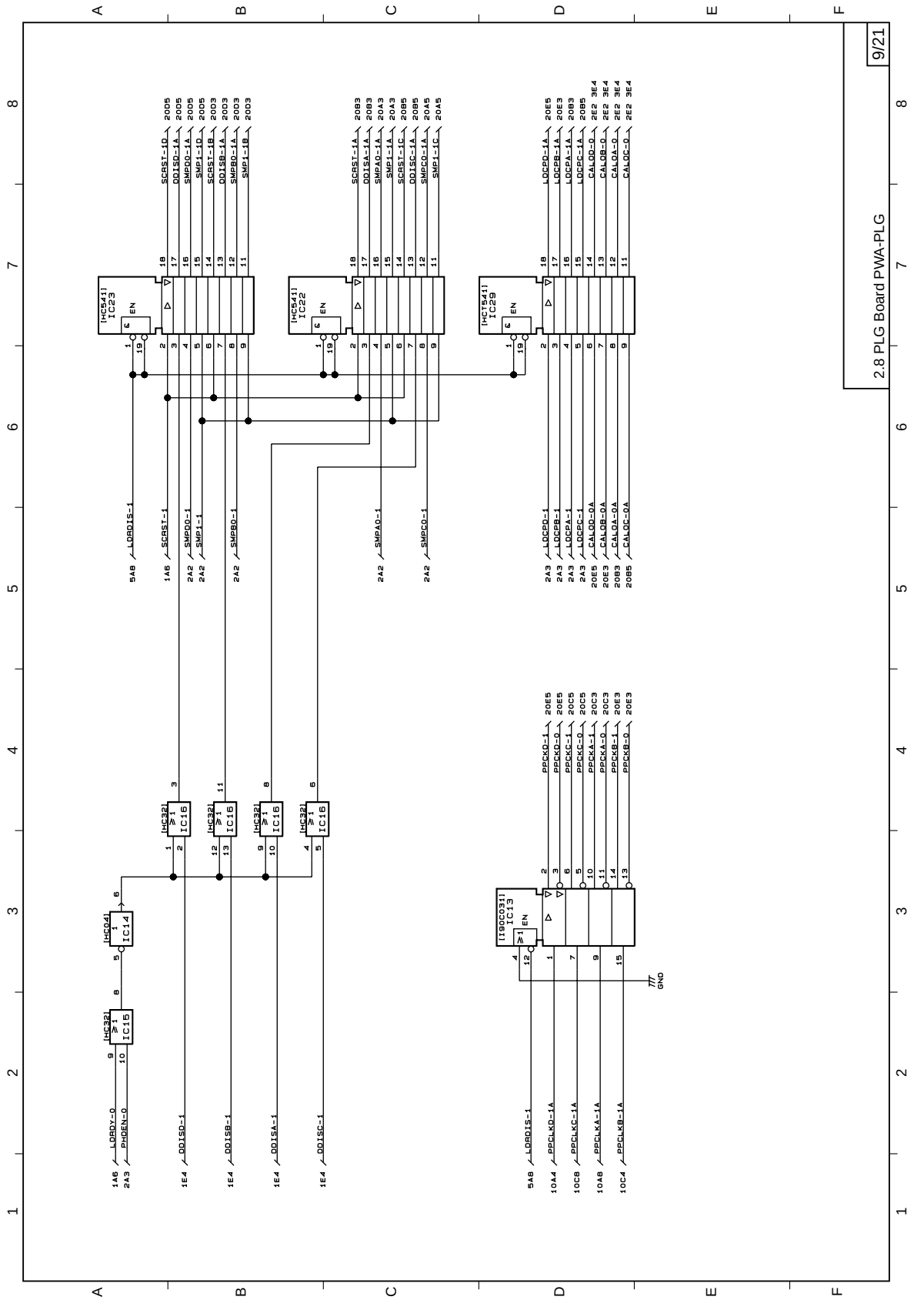

2.8 PLG Board PWA-PLG
4/21
SRAM32Kx8
M27C199
IC39
EPROM 64Kx16
M27C1024
IC40
EEPROM1K
M93C46S
IC51
7504P
IC52
1SS193
D3
R41
R42
R16
R17
R18
R19
C18
C39
VDD
GND
A[0:16]
D[0:15]
CSPROM-0
CSSRAM-0
RD-0
WR-0
CSNVM-0
SCLK-1
TXD-1
RXD-1

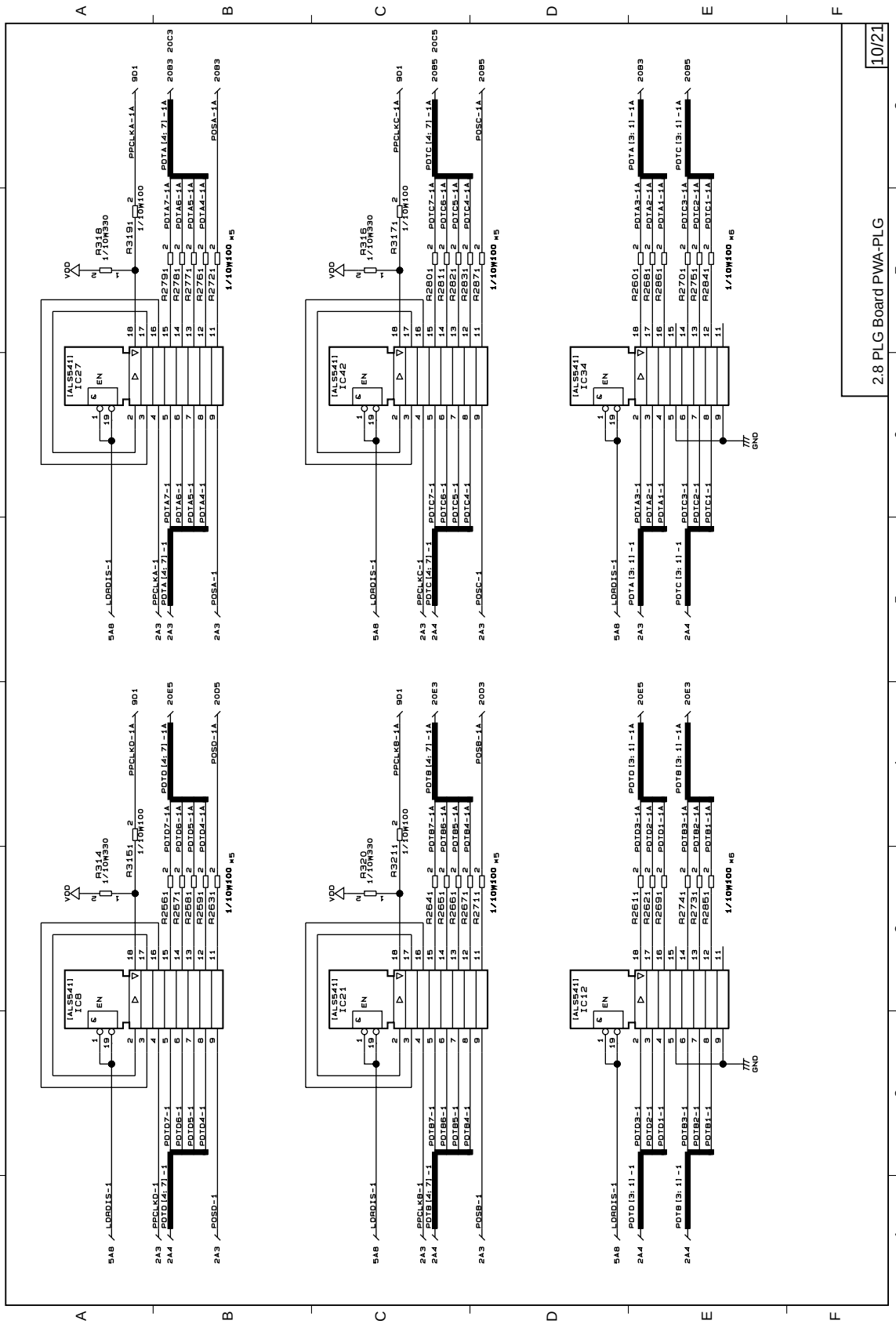

2.8 PLG Board PWA-PLG
5/21

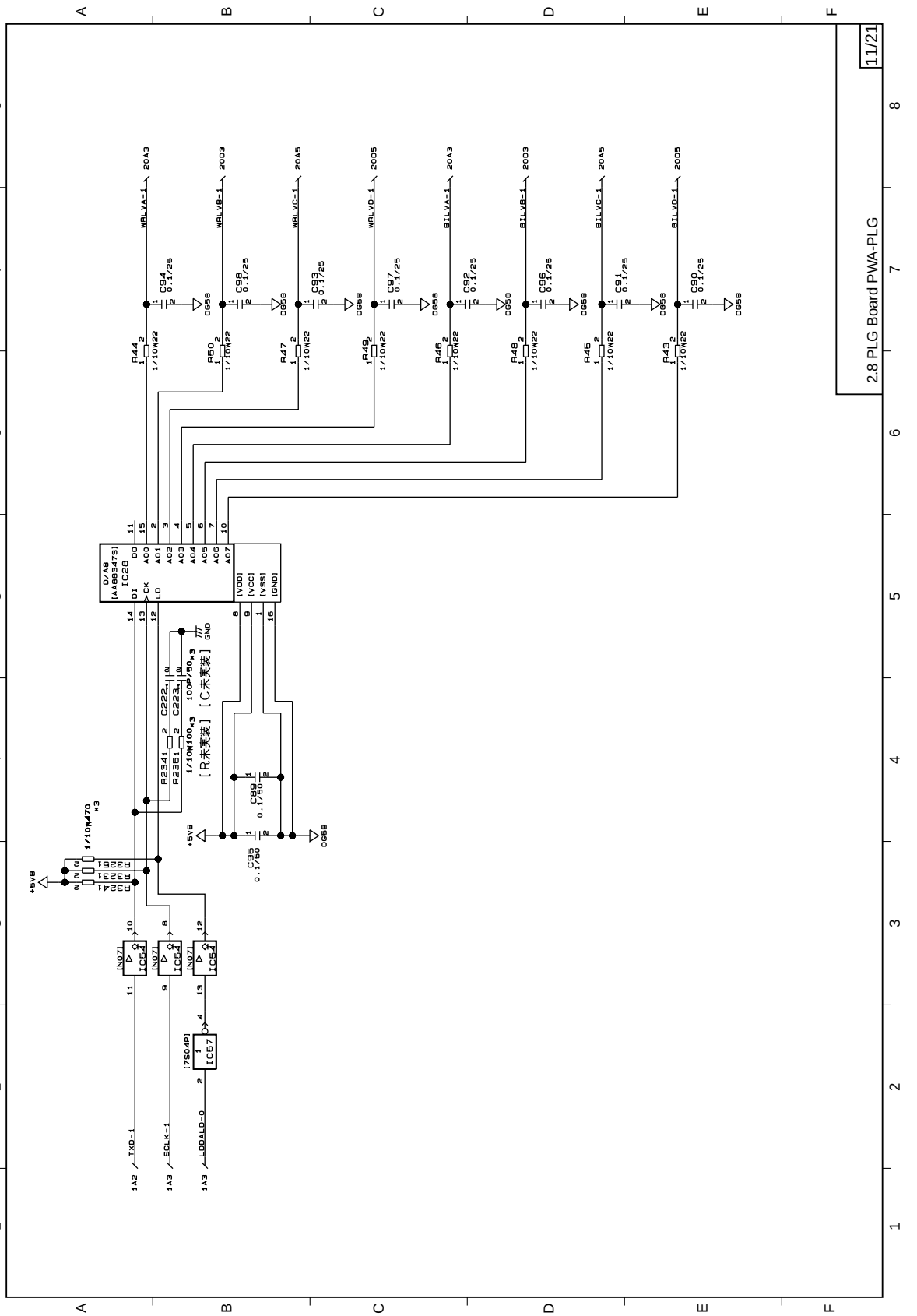

2.8 PLG Board PWA-PLG
6/21
[I C未実装]
IC4
IC5
IC3
IC2
[VHCT541]
[VHC541]
C103
C6
22P/50
220P/50
GND
VDD

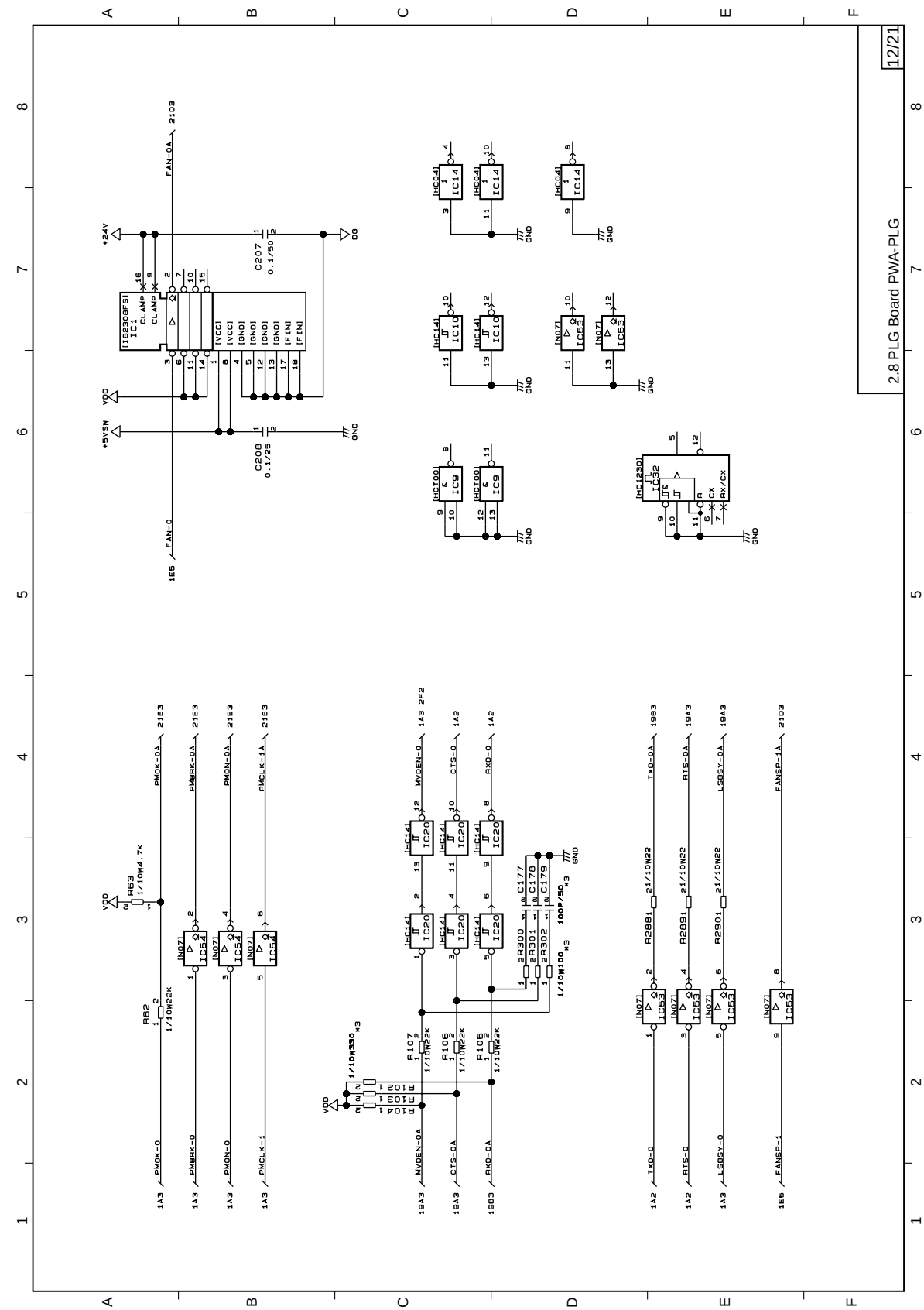

2.8 PLG Board PWA-PLG
7/21
[74C245] IC11
[HC244] IC25
[HC244] IC19
[74S04P] IC6
[7532P] IC7
1/10W4.7K
VDD
GND
CPUD0[0:7]-1
CPUA[0:15]-1
D[0:7]
A[0:15]
EWSCN-0
CSPOPS-0
RD-0
WR-0
CPURQ-0
CPUWR-0
CSPOP-0A

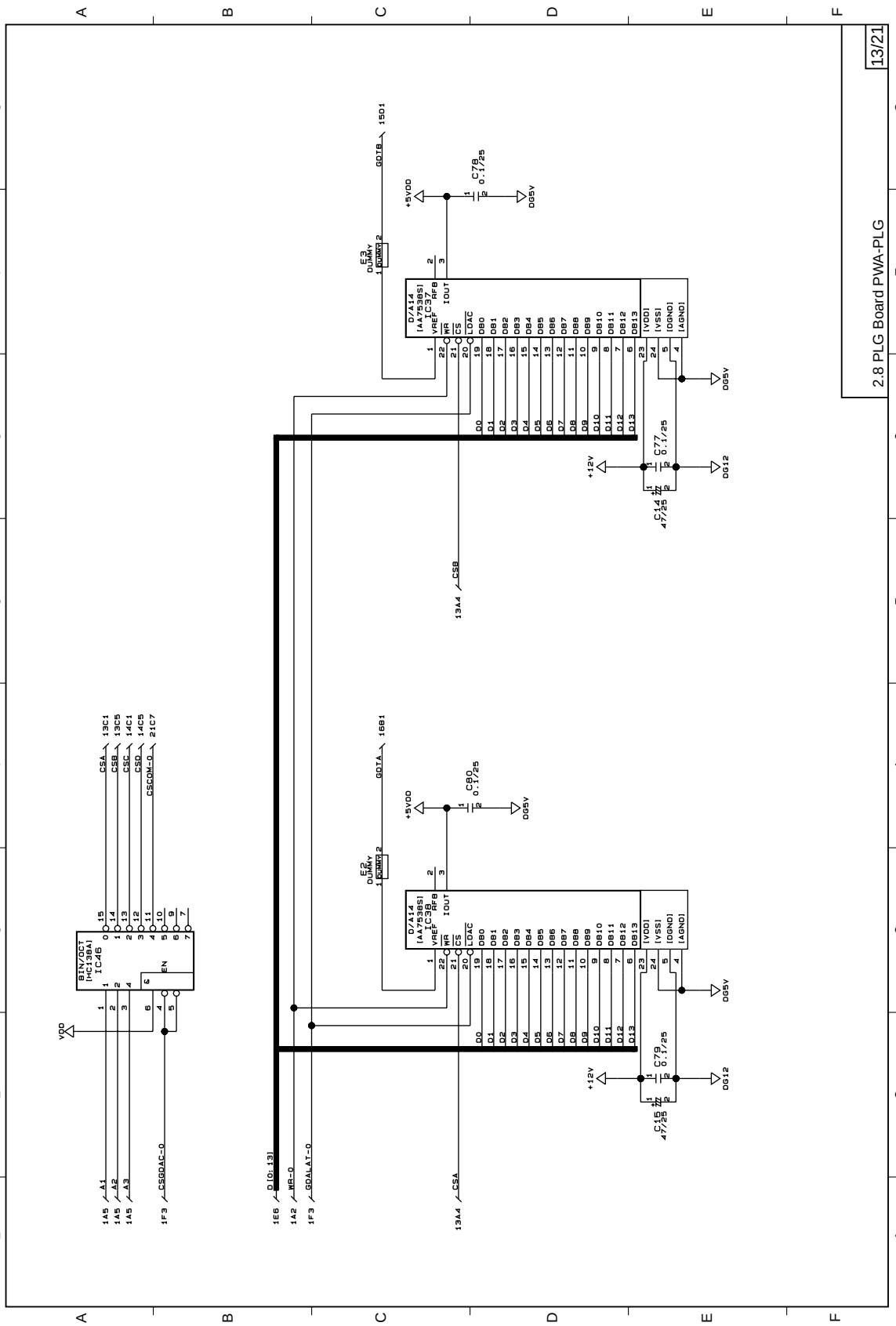

2.8 PLG Board PWA-PLG
8/21

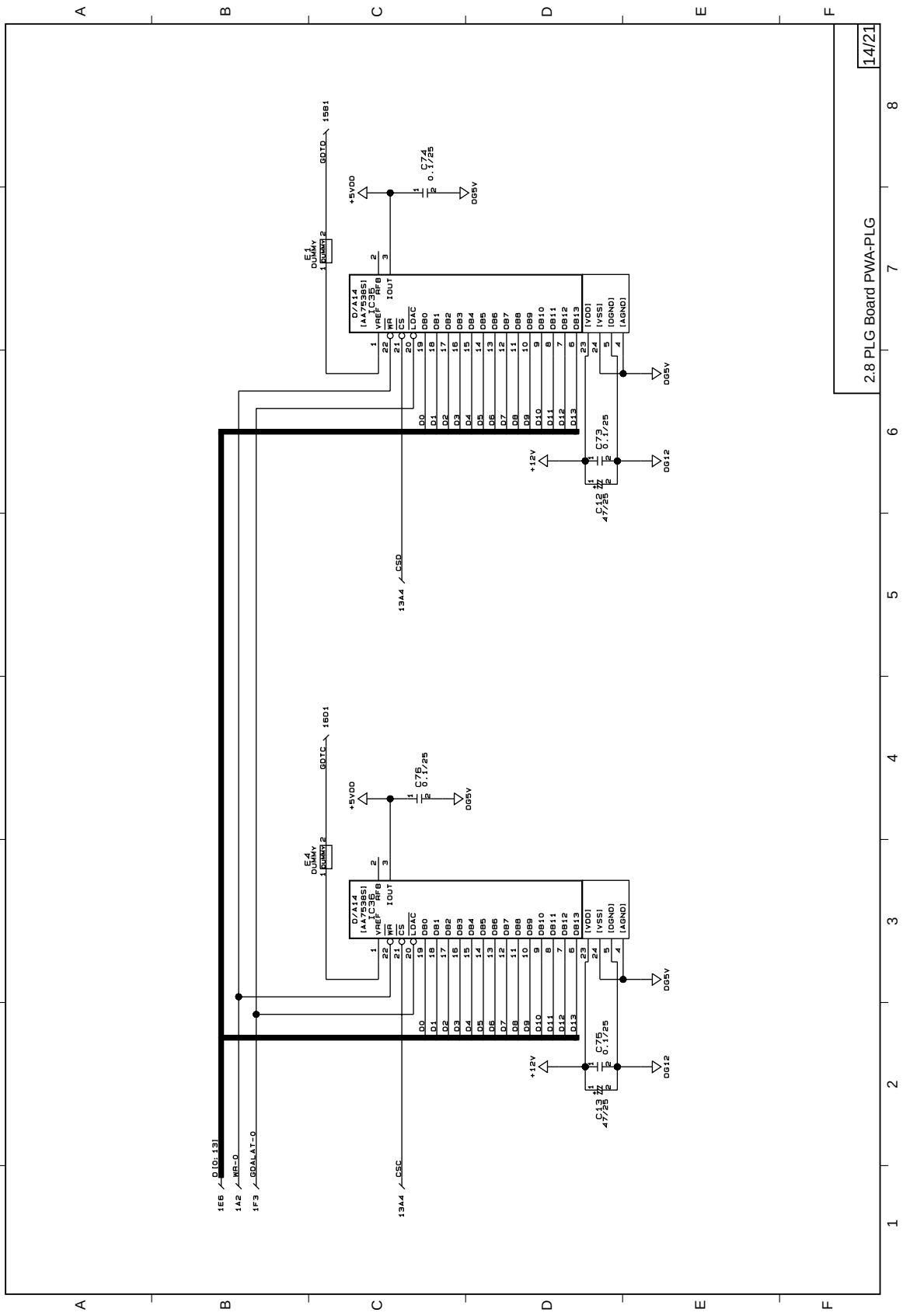

2.8 PLG Board PWA-PLG
9/21
IHC541
IC23
IHC541
IC22
IHCT541
IC29
IHC32
IC16
IHC04
IC14
IHC32
IC15
I19CC031
IC13
LOBDY-0
PHDEN-0
LOBDIS-1
SCRST-1
SMPDO-1
SMP1-1
SMPBO-1
SMPAO-1
SMPCO-1
DDISD-1
DDISB-1
DDISA-1
DDISC-1
LOCPD-1
LOCPB-1
LOCPA-1
LOCPC-1
CALOD-0A
CALOB-0A
CALOA-0A
CALOC-0A
PPCKD-1
PPCKD-0
PPCKC-1
PPCKC-0
PPCKA-1
PPCKA-0
PPCKB-1
PPCKB-0
PPCLKD-1A
PPCLKC-1A
PPCLKA-1A
PPCLKB-1A
GND

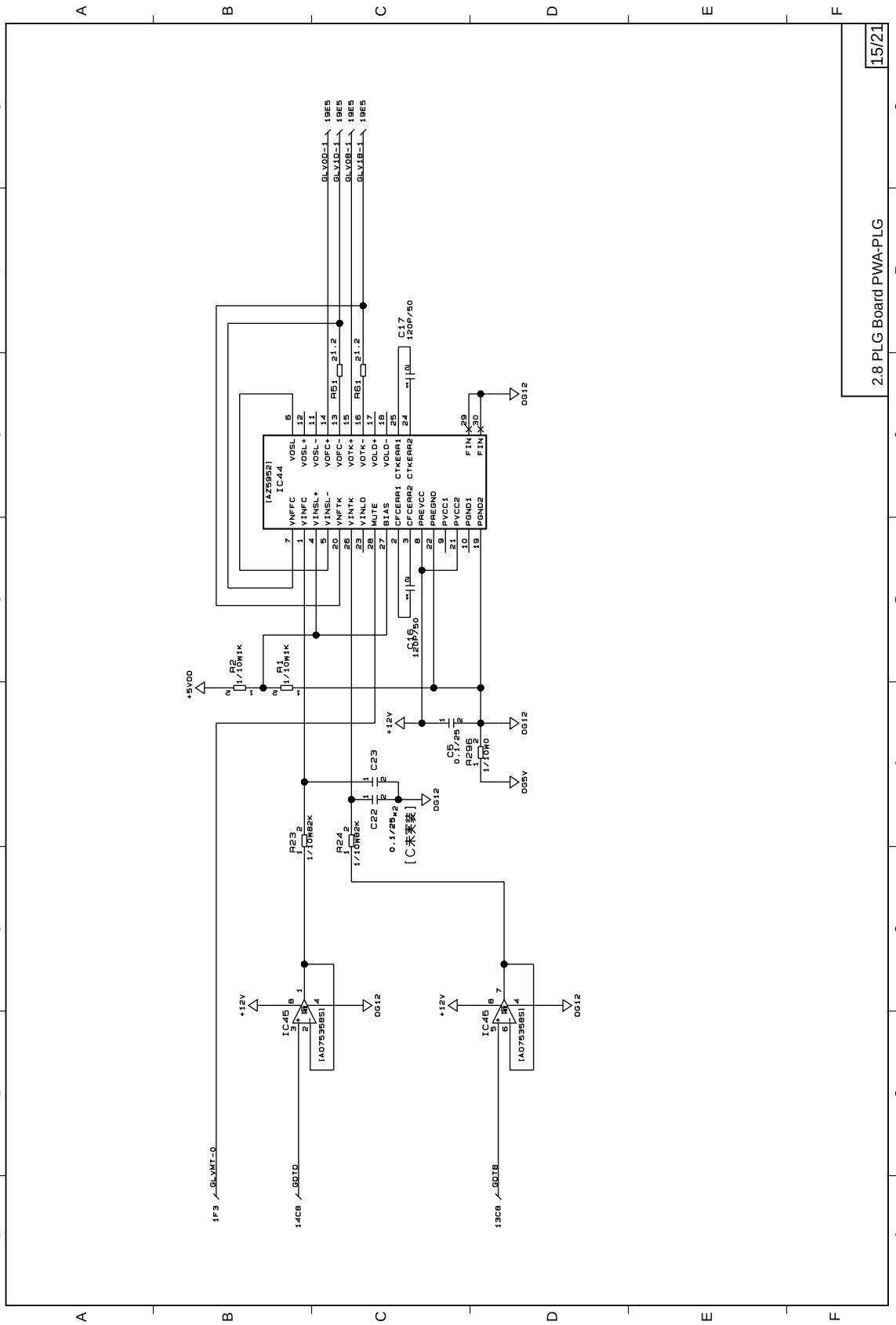

2.8 PLG Board PWA-PLG
10/21

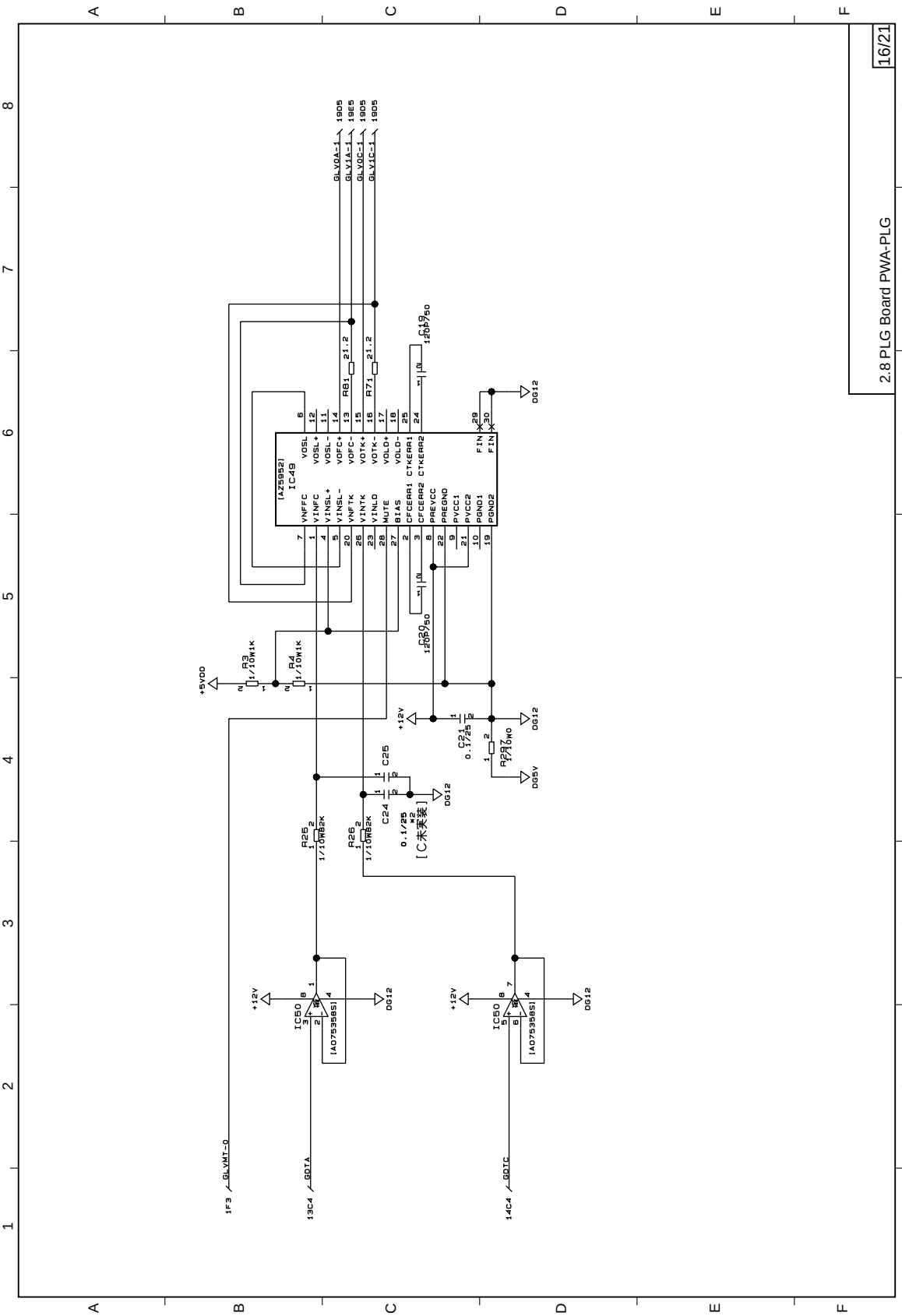

2.8 PLG Board PWA-PLG
11/21
D/A8
IAA883475I
IC28
[R未実装] [C未実装]
1/10M470 ×3
1/10M100 ×3
100P/50 ×3
R2341
R2351
C2221
C2231
C95 0.1/50
C98 0.1/50
R44 1/10M22
R50 1/10M22
R47 1/10M22
R49 1/10M22
R46 1/10M22
R48 1/10M22
R45 1/10M22
R43 1/10M22
C94 0.1/25
C98 0.1/25
C93 0.1/25
C97 0.1/25
C92 0.1/25
C96 0.1/25
C91 0.1/25
C90 0.1/25
WBLYA-1
WBLYB-1
WBLYC-1
WBLYD-1
BILYA-1
BILYB-1
BILYC-1
BILYD-1
2043
2003
2045
2005
+5VB
DGSB
GND
TXD-1
SCLK-1
LODALD-0
IN07
LC54
I7504PI
IC57

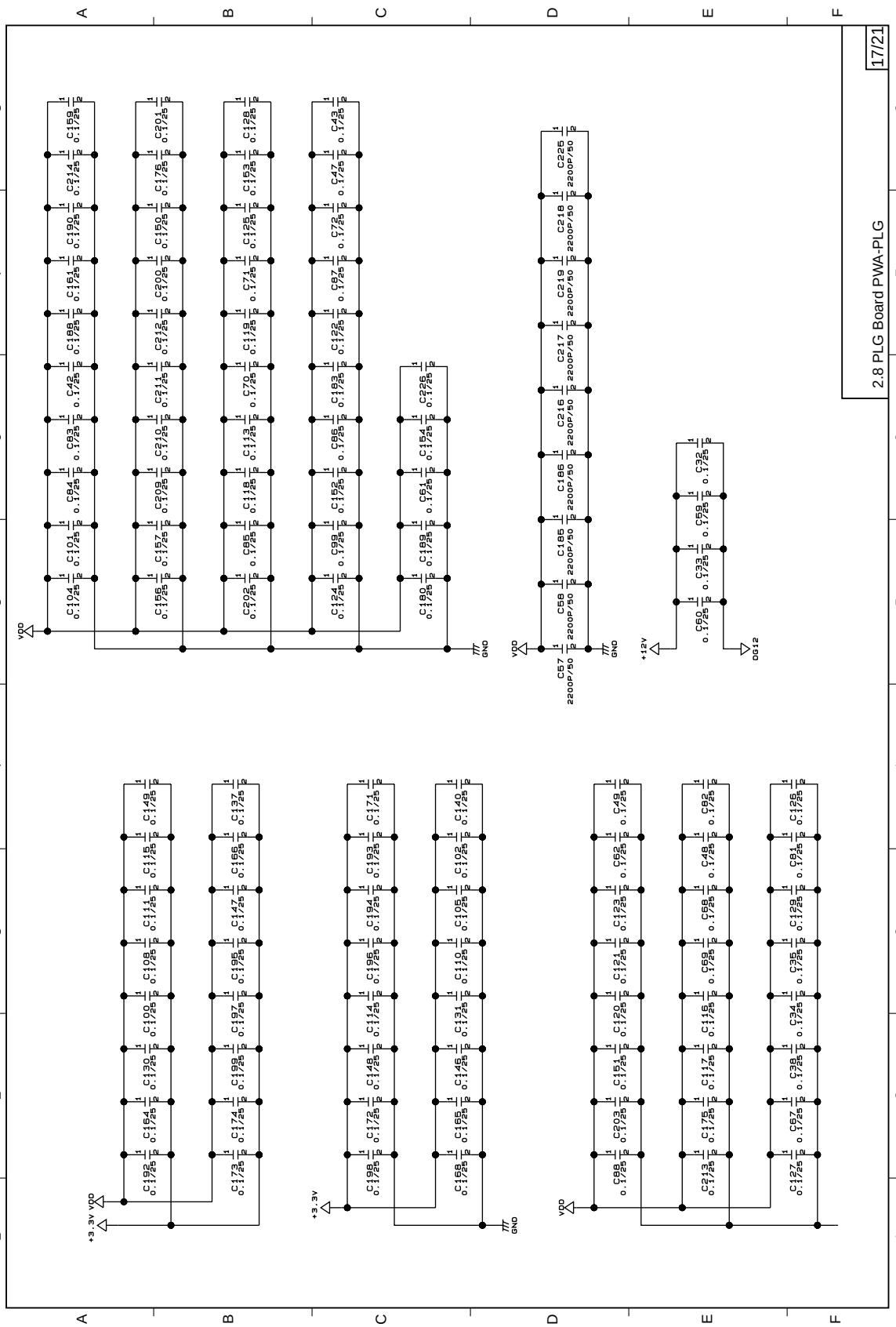

2.8 PLG Board PWA-PLG
12/21

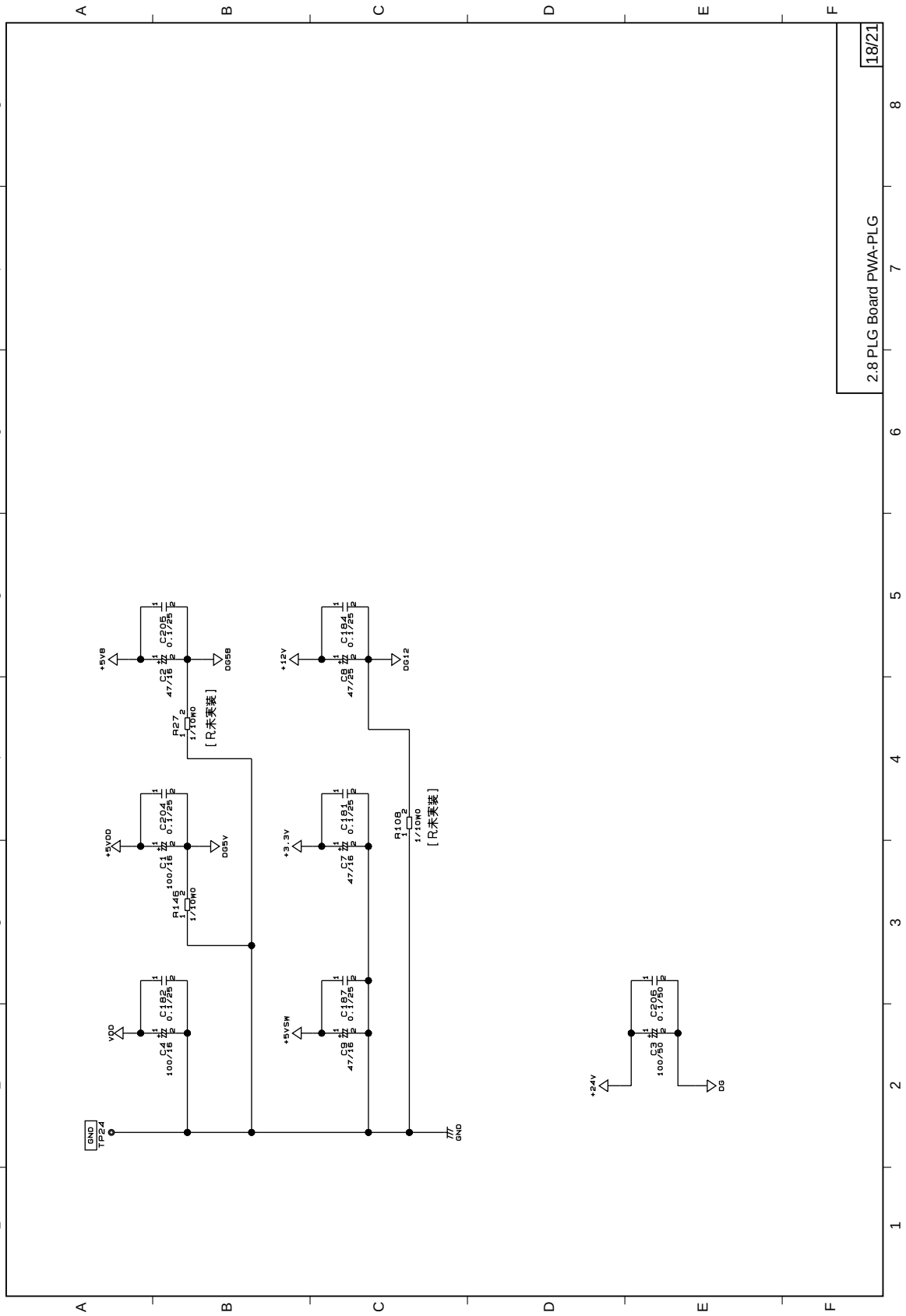

2.8 PLG Board PWA-PLG
13/21
BIN/OCT (ACT138) IC46
D/A14 (AA7538S) IC37
D/A14 (AA7538S) IC38
+5VDD
+12V
DGSV
DG12
D[0:13]
WR-0
GDALAT-0
CSA
CSB
CSC
CSD
CSCOM-0
CSGDAC-0
GDTA
GDTB
C77 0.1/25
C78 0.1/25
C79 0.1/25
C80 0.1/25
C14 47/25
C15 47/25

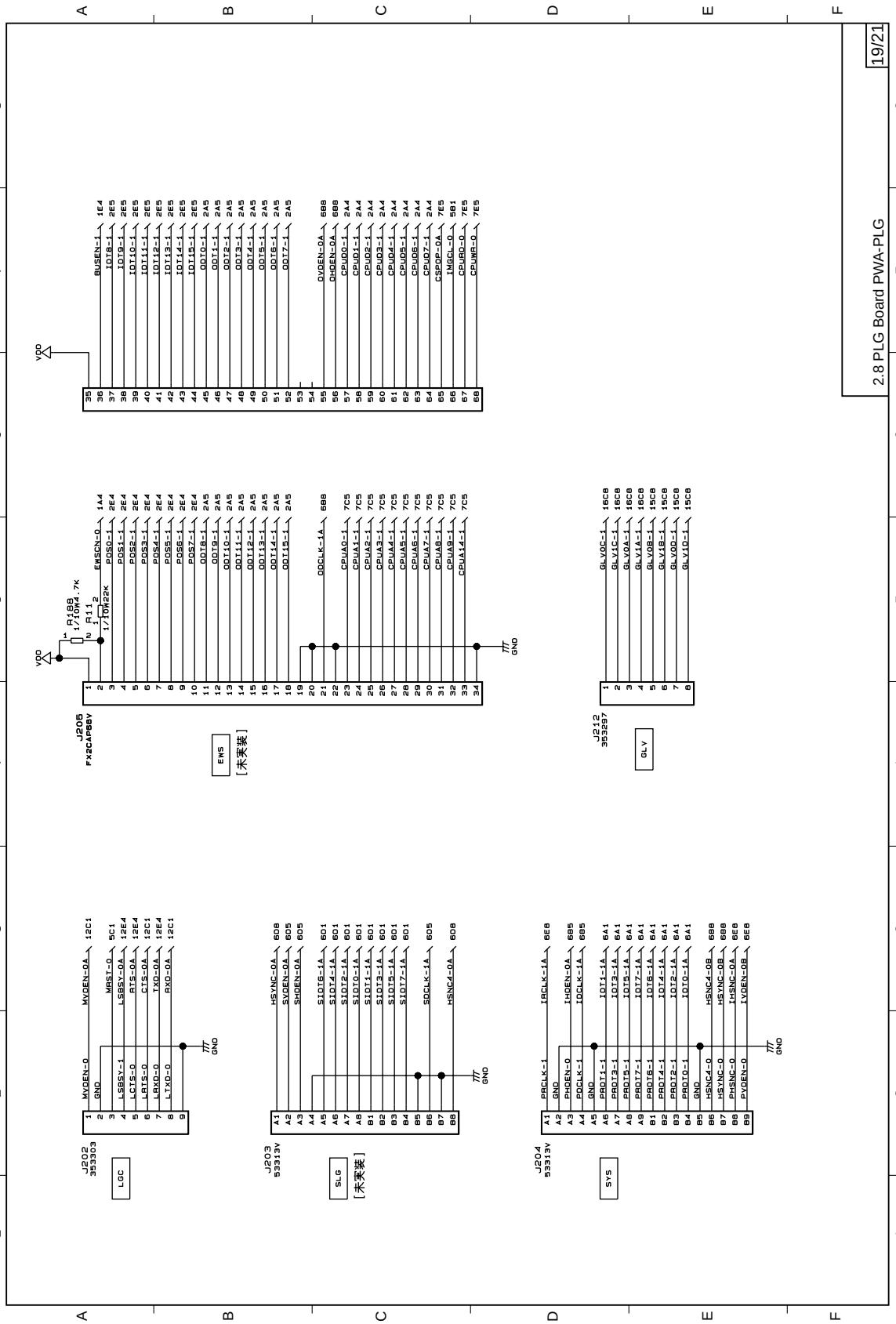

2.8 PLG Board PWA-PLG
14/21
D/A14
(AA7538S)
VREF RFB
WR IOUT
CS
LDAC
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13
(VDD) (VSS) (DGND) (AGND)
E4
DUMMY
+5VDD
+12V
DG5V
DG12
C74 0.1/25
C73 0.1/25
C75 0.1/25
C13 47/25
GDIO
1581
1601
D[0:13]
WR-0
GDALAT-0
CSD
CSC
1E6
1A2
1F3
13A4

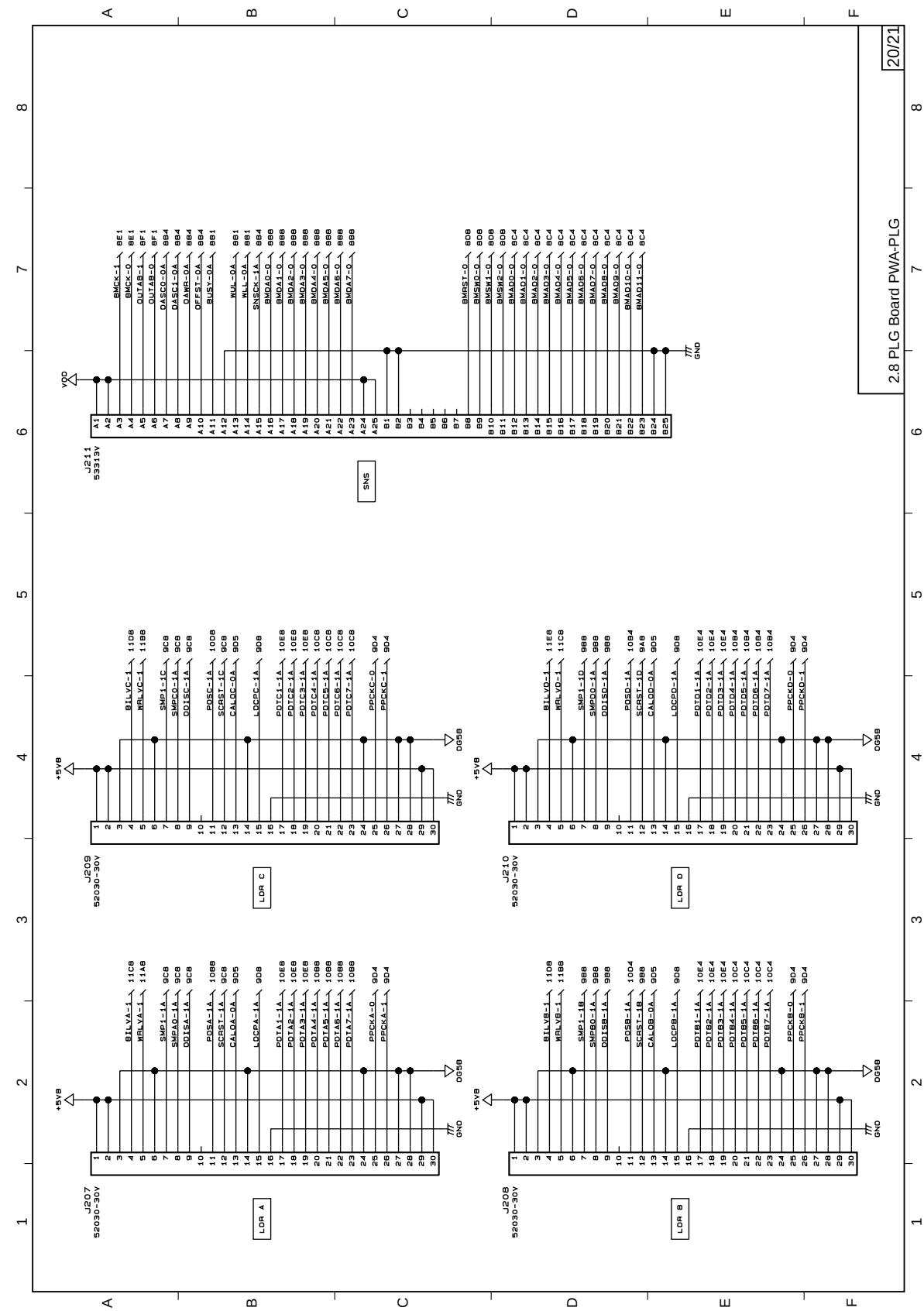

2.8 PLG Board PWA-PLG
15/21
IC44
IAZ59521
VOSL
VOSL+
VOSL-
VOFC+
VOFC-
VOTK+
VOTK-
VOLO+
VOLO-
CTKEAR1
CTKEAR2
FIN
VNFFC
VINFC
VINSL+
VINSL-
VNFTK
VINTK
VINLO
MUTE
BIAS
PREGND
PVCC1
PVCC2
PGND1
PGND2
GLY0D-1
GLY1D-1
GLY0B-1
GLY1B-1
R51
R61
C17
C19
C5
R296
C23
C22
R23
R24
IC45
IA07538BS
+5VDD
+12V
DG12
DG5V
GLYMT-0
GDTD
GDTB

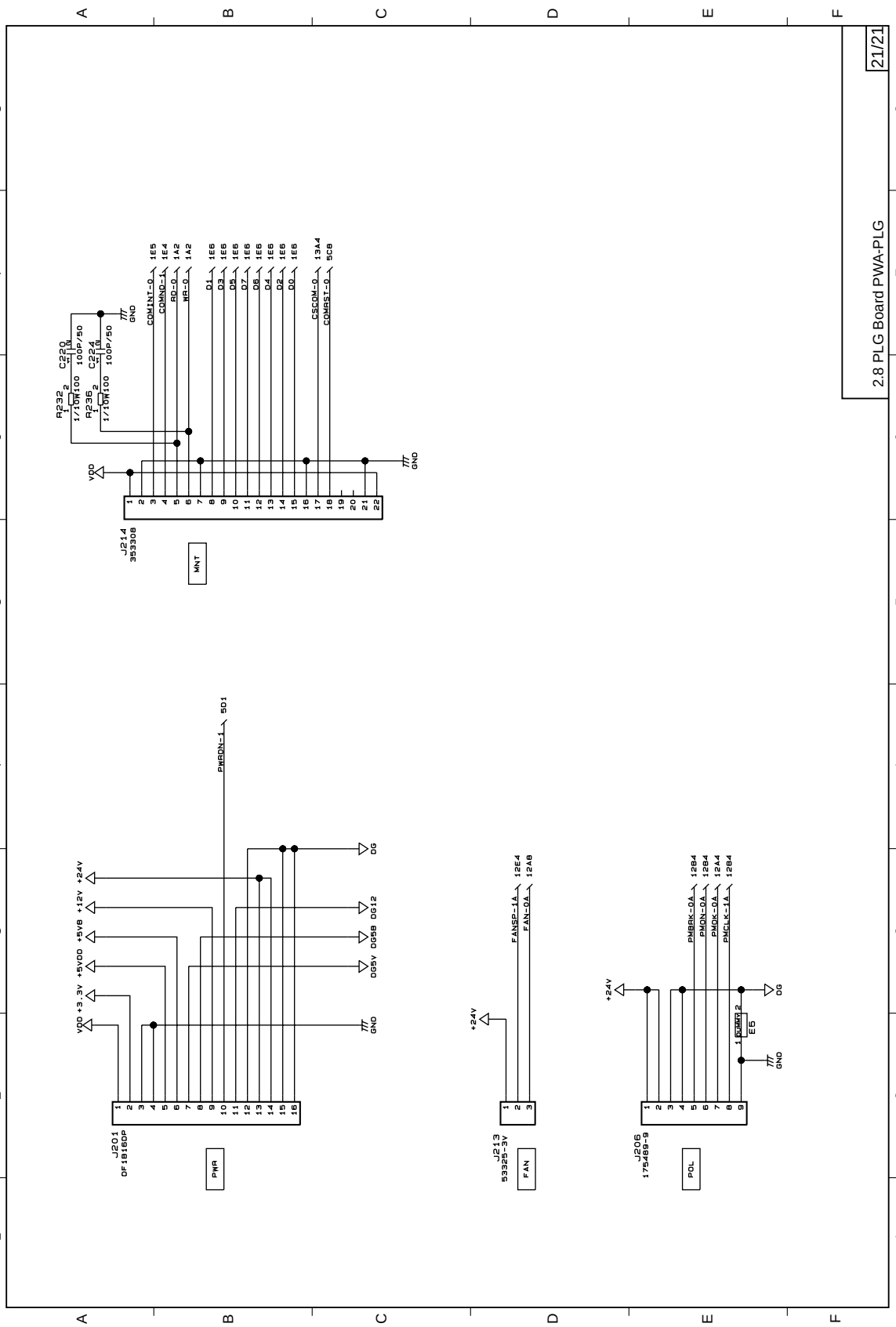

2.8 PLG Board PWA-PLG
16/21
IC49
[AZ5952]
VNFFC
VINFC
VINSL+
VINSL-
VNFTK
VINTK
VINLD
MUTE
BIAS
CFCERR1
CFCERR2
PREVCC
PREGND
PVCC1
PVCC2
PGND1
PGND2
VOSL
VOSL+
VOSL-
VOFC+
VOFC-
VOTK+
VOTK-
VOLD+
VOLD-
CTKERR1
CTKERR2
FIN
GLV0A-1
GLV1A-1
GLV0C-1
GLV1C-1
R81 21.2
R71 21.2
+5VDD
+12V
DG12
DG5V
R3 1/10W1K
R4 1/10W1K
C29 1/25V50
C19 1/25V50
C21 0.1/25
R27 1/10W0
C25
C24 0.1/25 *2 [C未実装]
R25 1/10W82K
R26 1/10W82K
IC50 [AO7538BS]
GLVM7-0
GDTA
GDTC


2.8 PLG Board PWA-PLG
17/21

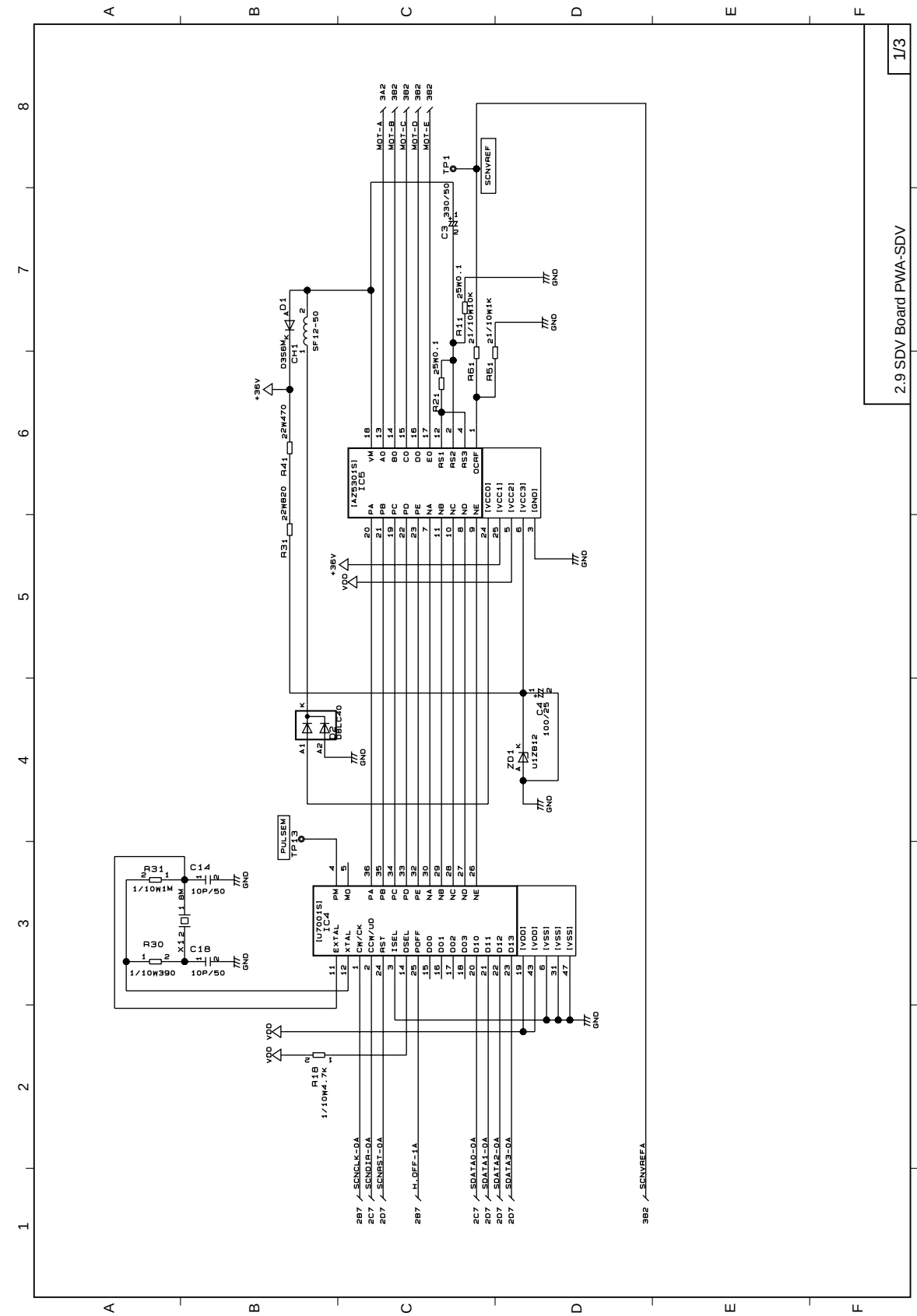

2.8 PLG Board PWA-PLG
18/21
GND
TP24
VDD
+5VDD
+5VSW
+3.3V
+12V
+24V
+5VB
DGSV
DGSB
DG12
DG
GND
C4 100/16
C182 0.1/25
C1 100/16
C204 0.1/25
C2 47/16
C205 0.1/25
C5 47/16
C187 0.1/25
C7 47/16
C184 0.1/25
C8 47/25
C184 0.1/25
C3 100/50
C206 0.1/50
R146 1/10WΩ
R27 1/10WΩ
R108 1/10WΩ
[R未実装]
[R未実装]

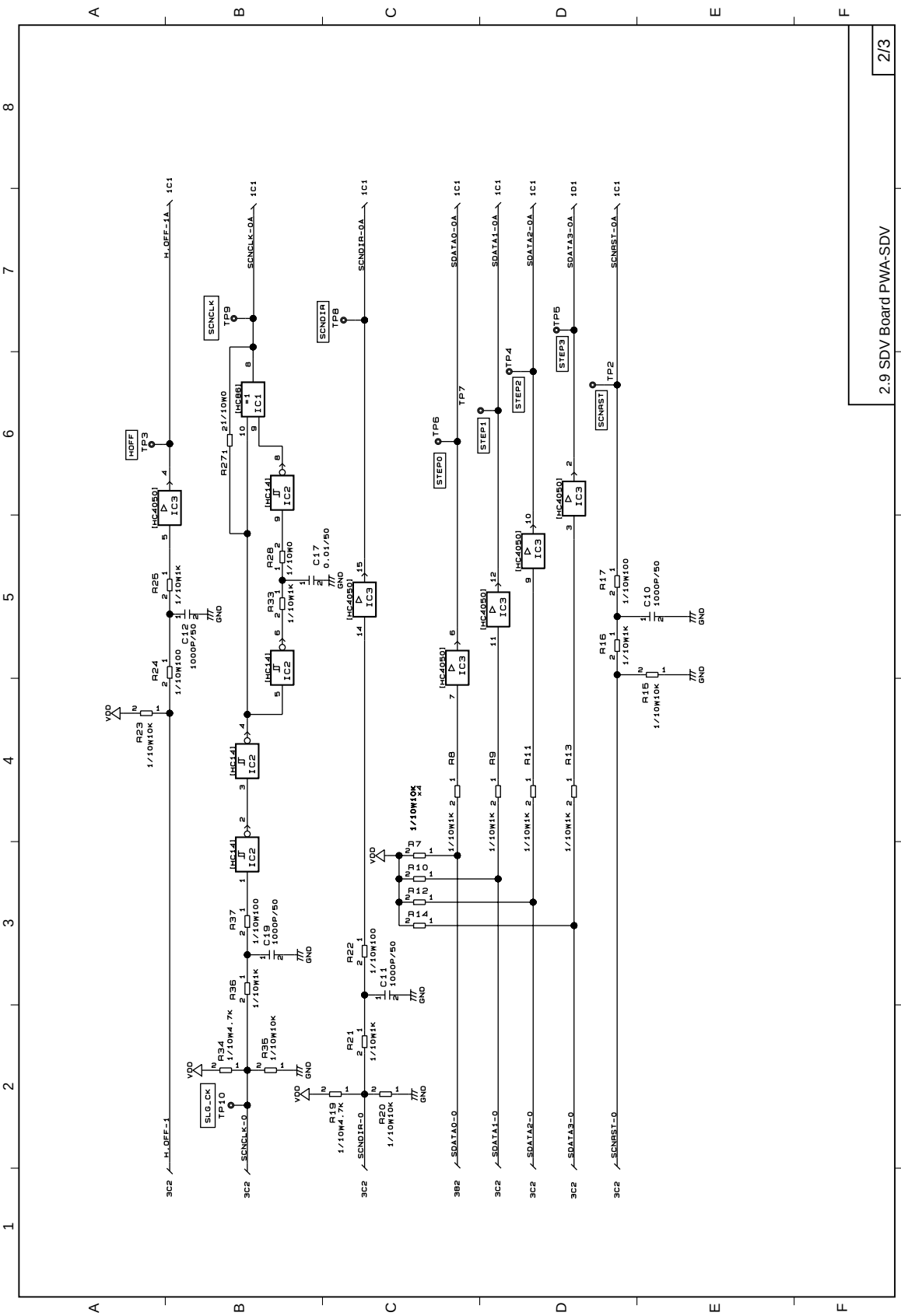

2.8 PLG Board PWA-PLG
19/21
J205
FX2CLAPSGV
J202
355303
LGC
J203
53313V
SLG
[未実装]
J204
53313V
SYS
J212
353297
GLV
EMS
[未実装]
R108
1/10W4.7K
R11
1/10W22K
VDD
GND

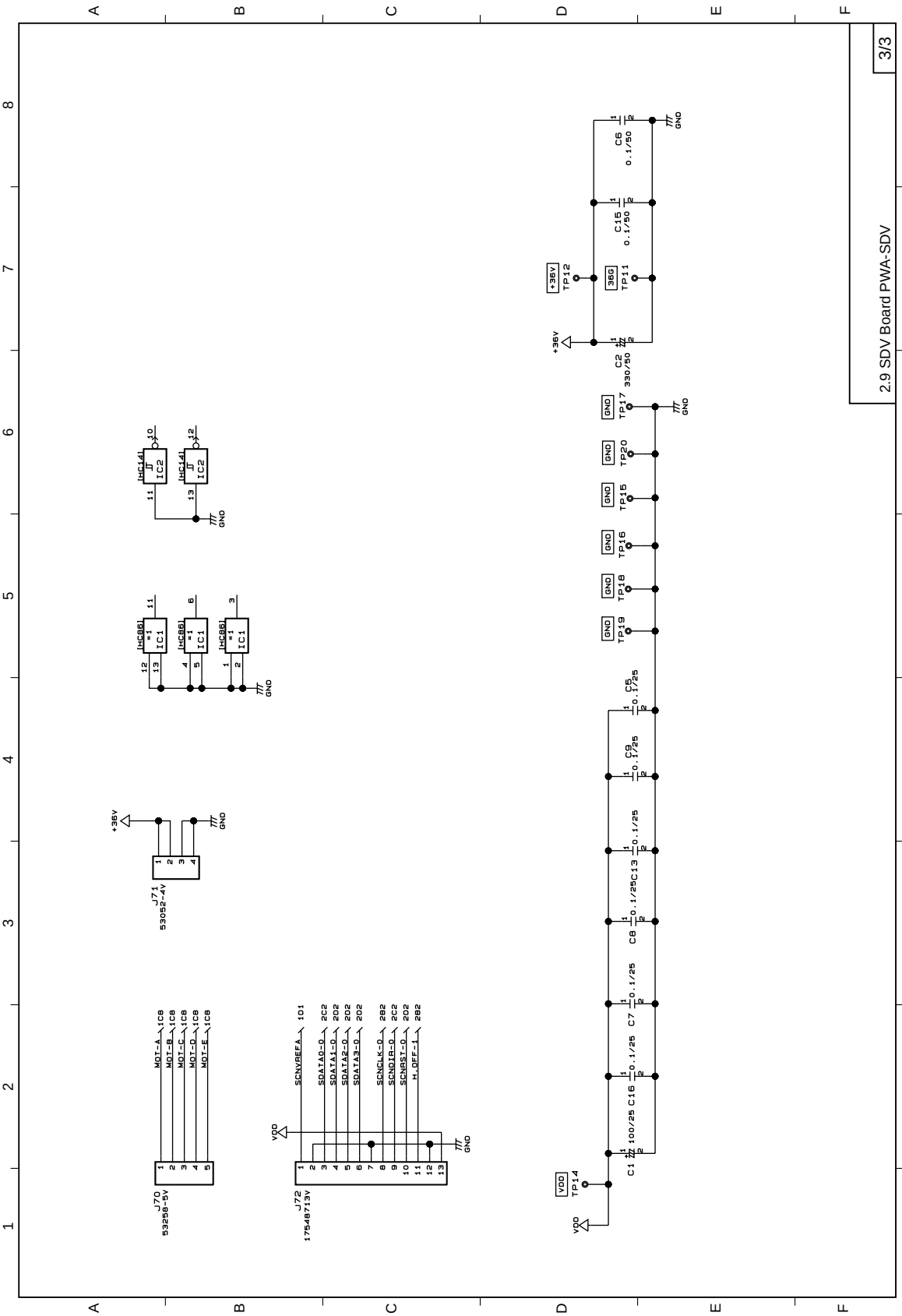

2.8 PLG Board PWA-PLG
20/21
J207
52030-30V
LDR A
J208
52030-30V
LDR B
J209
52030-30V
LDR C
J210
52030-30V
LDR D
J211
53313V
SNS
+5VB
GND
VDD
0058


2.8 PLG Board PWA-PLG
21/21
J214
395308
MNT
J201
DF18(8.0)P
PWR
J213
53326-3Y
FAN
J206
175489-9
POL
R232
1/10W100
C220
100P/50
R236
1/10W100
C224
100P/50
VDD
GND
COMINT-O
COMND-1
RD-O
WR-O
D1
D3
D5
D7
D6
D4
D2
D0
CSCOM-O
COMRST-O
PWRON-1
+3.3V
+5VDD
+5VB
+12V
+24V
DG5V
DG5B
DG12
DG
FANSP-1A
FAN-0A
PMBRK-0A
PMON-0A
PMDK-0A
PMCLK-1A
CONN 2

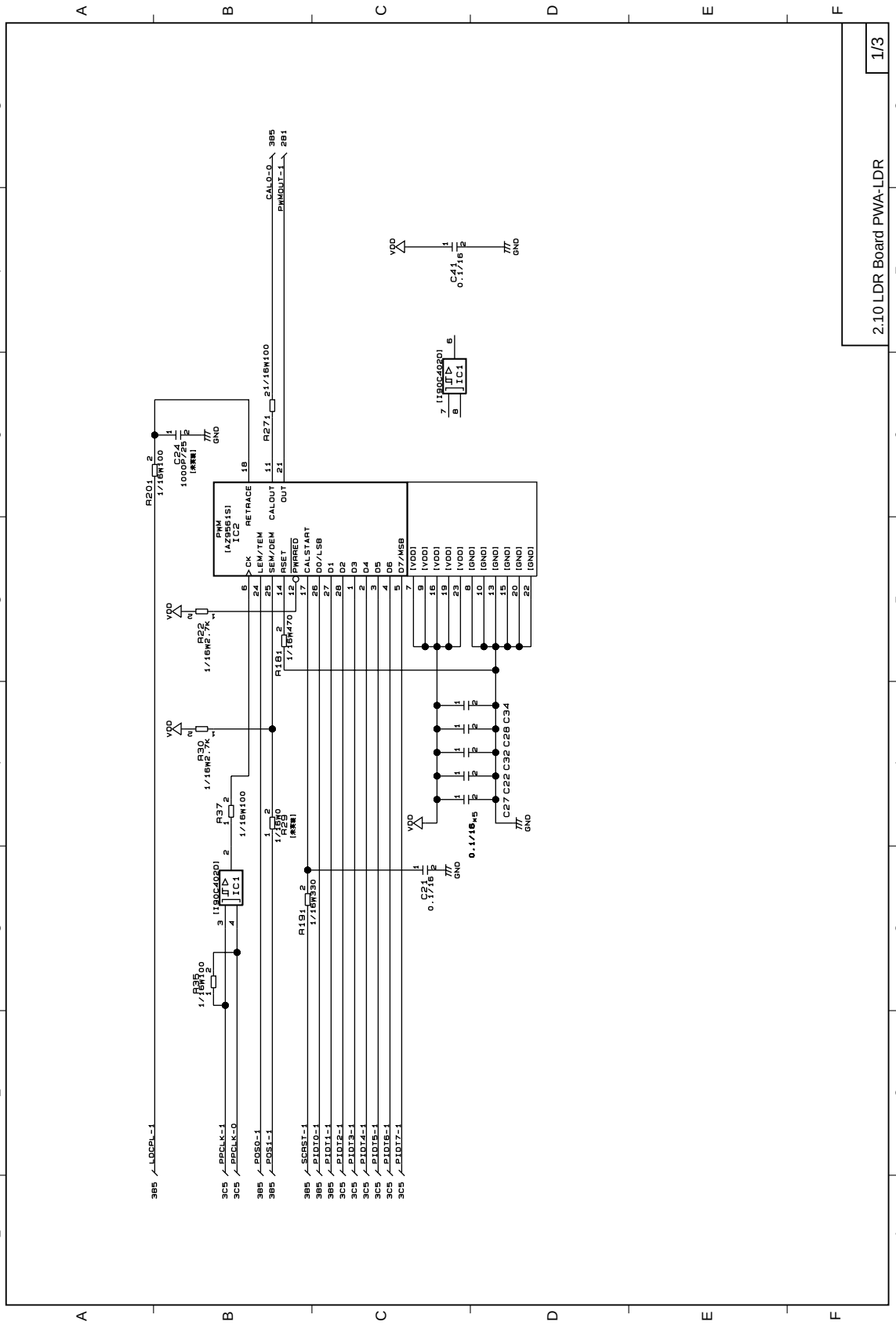
2.9 SDV Board (PWA-SDV) 1/3~3/3

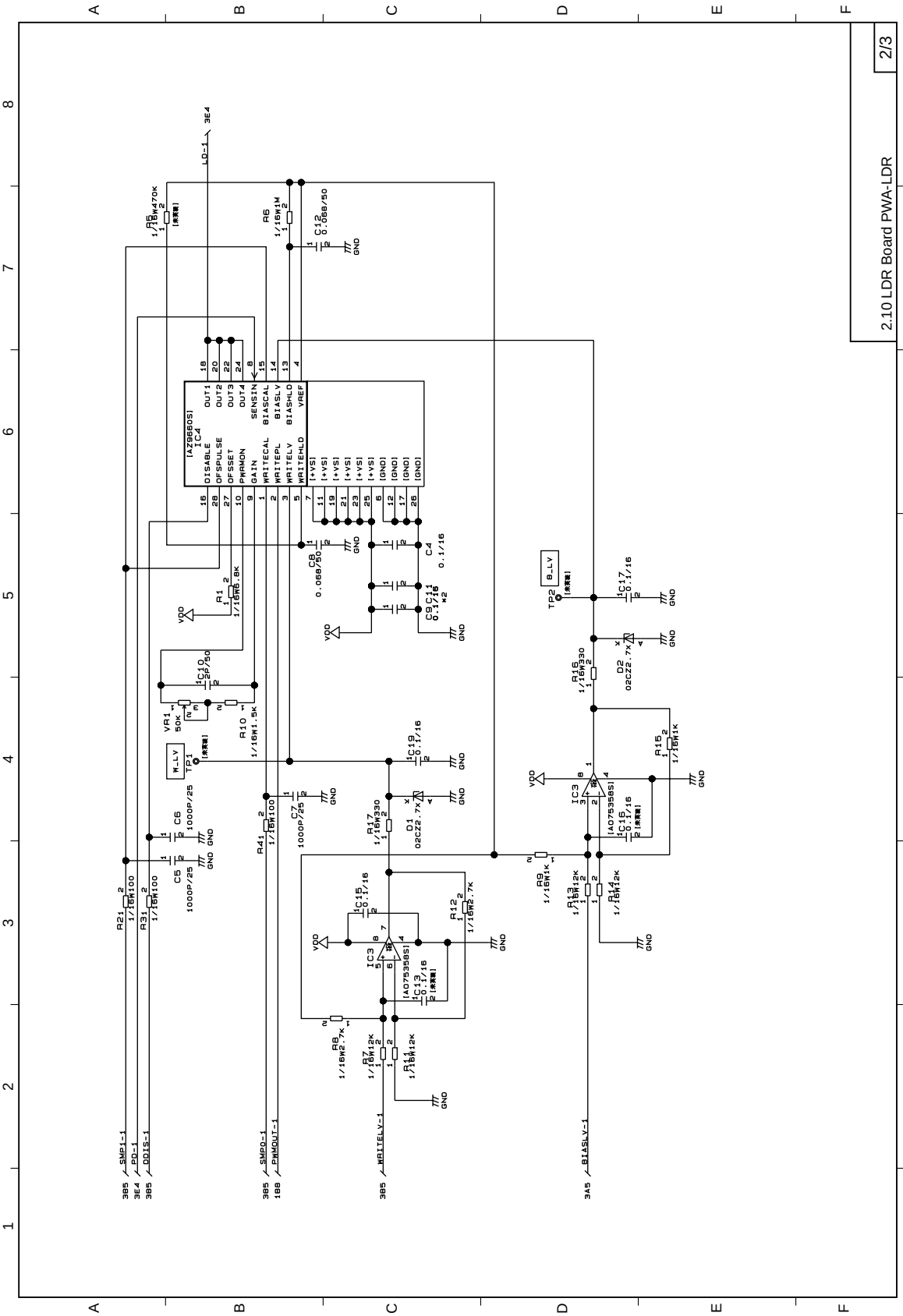


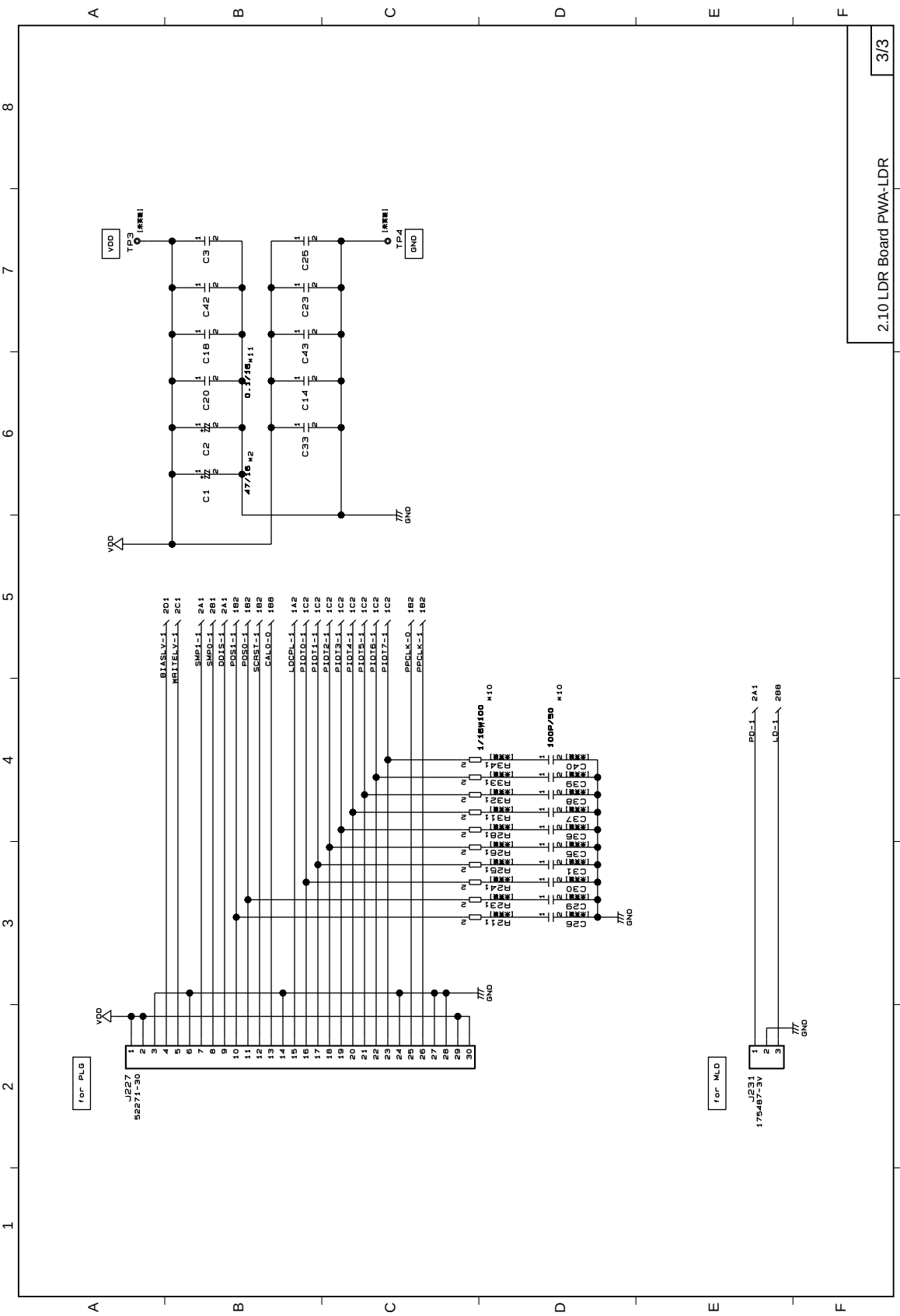

2.9 SDV Board PWA-SDV
2/3


2.9 SDV Board PWA-SDV
3/3
+36V
GND
VDD
J70
53259-5V
J71
53052-4V
J72
1754871-3V
MOT-A
MOT-B
MOT-C
MOT-D
MOT-E
SCNVREFA
SDATA0-0
SDATA1-0
SDATA2-0
SDATA3-0
SCNCLK-0
SCNDIR-0
SCNRST-0
H.OFF-1
C1
C2
C5
C6
C7
C8
C9
C13
C15
C16
TP11
TP12
TP14
TP15
TP16
TP17
TP18
TP19
TP20

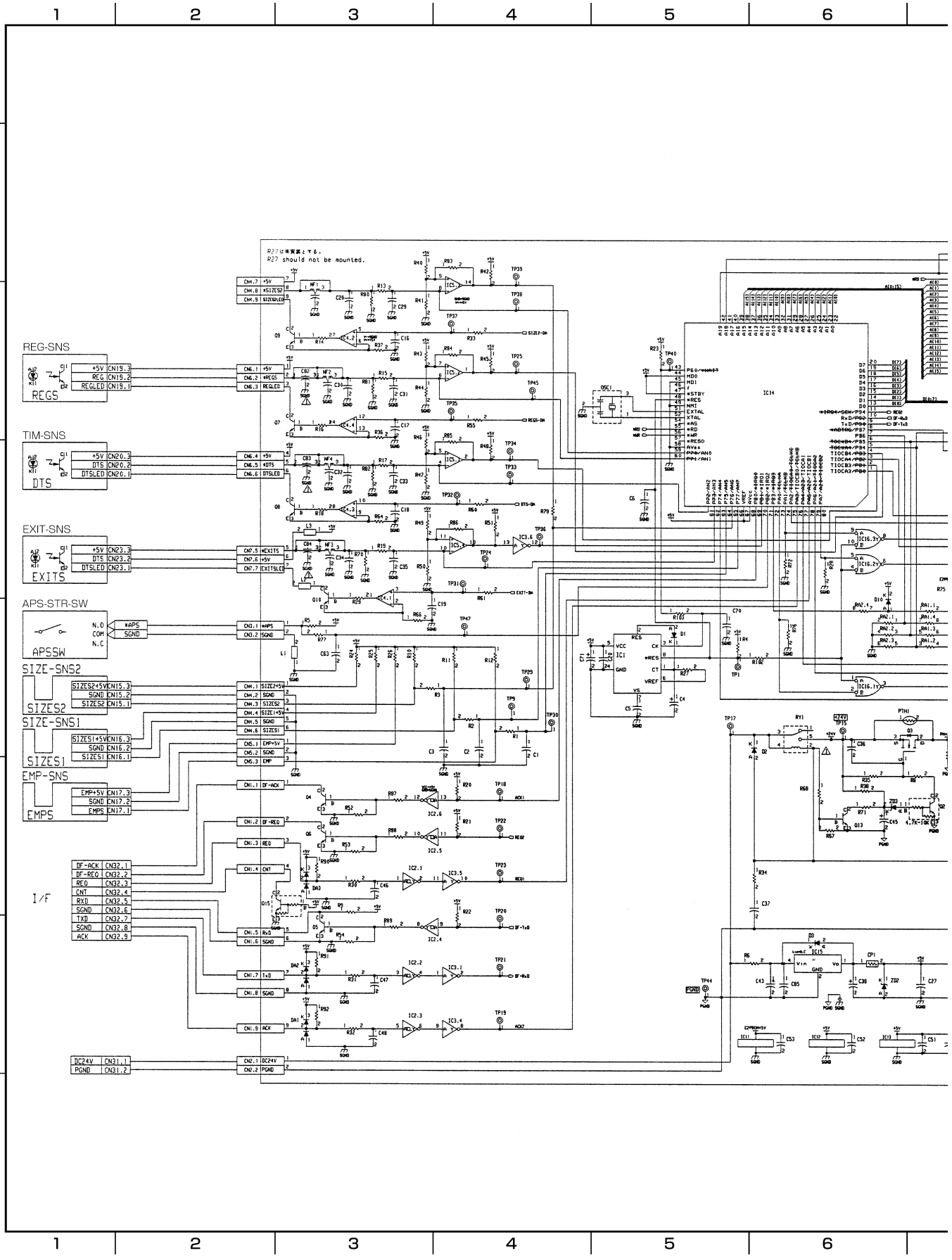
2.10 LDR Board (PWA-LDR) 1/3~3/3

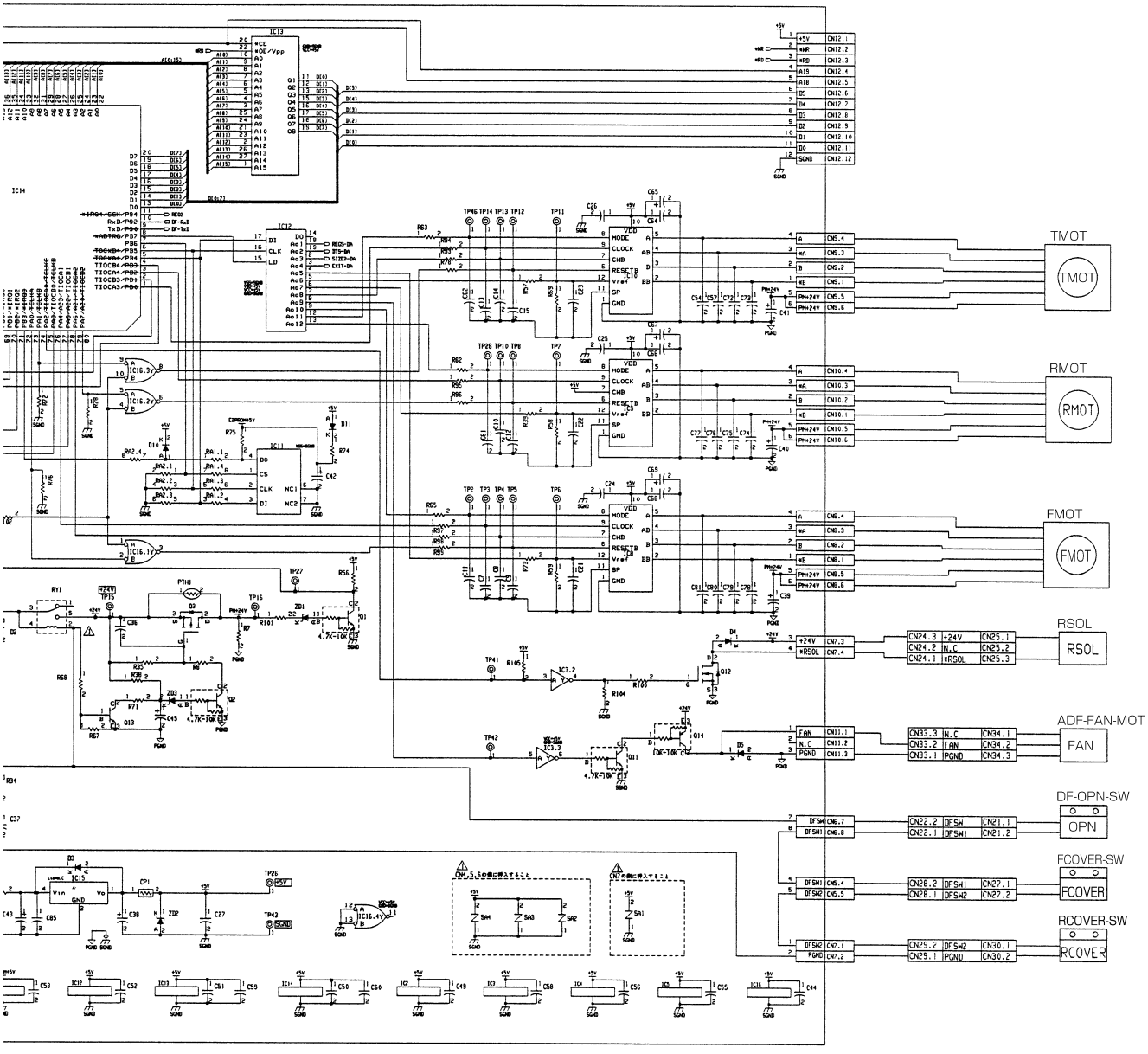



2.10 LDR Board PWA-LDR
2/3


2.10 LDR Board PWA-LDR
3/3
for PLG
for MLD
J227
52271-30
J231
175487-3V
VDD
GND
TP3
TP4
BIASLV-1
WRITELV-1
SWP1-1
SWP0-1
ODIS-1
PDS1-1
PDS0-1
SCRST-1
CALO-0
LOCPL-1
PIOI0-1
PIOI1-1
PIOI2-1
PIOI3-1
PIOI4-1
PIOI5-1
PIOI6-1
PIOI7-1
PPCLK-0
PPCLK-1
PD-1
LD-1
1/16W100
100P/50
0.1/16
47/16

2.11 ADF Circuit




TMOT
RMOT
FMOT
RSOL
ADF-FAN-MOT
DF-OPN-SW
FCOVER-SW
RCOVER-SW

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